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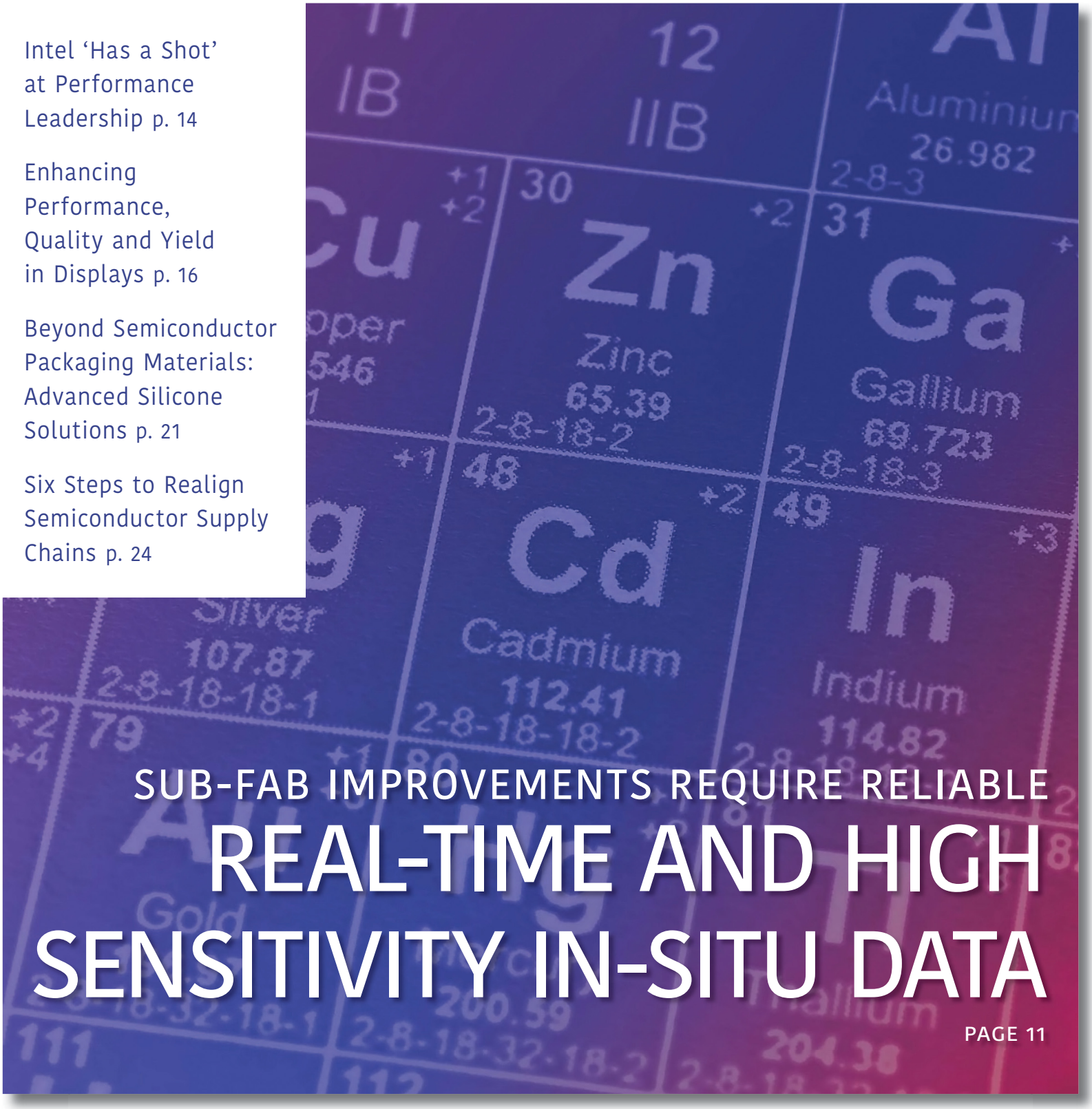
SEMICONDUCTOR DIGEST

NEWS AND INDUSTRY TRENDS

APRIL/MAY 2022



SUB-FAB IMPROVEMENTS REQUIRE RELIABLE

REAL-TIME AND HIGH SENSITIVITY IN-SITU DATA

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The **Technology Leadership Series** of the Americas is a collection of eight major events representing the various technology communities in our industry. These programs connect 2,400+ member companies and over 1.3 million global professionals to advance the technology and business of electronics manufacturing and the design-supply chain.

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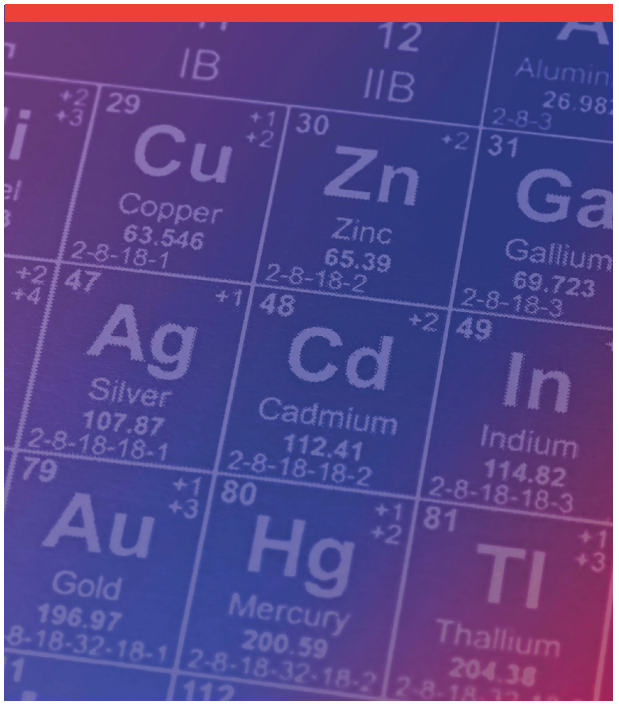
April/May 2022 | Volume 4 Number 3



COVER: Sub-fab applications have been seeing a resurgence as increased vacuum intensity and control along with new safety requirements from advanced process chemistry and related safety and abatement sustainability. *Source: Atonarp.*

Columns

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Editorial

$1 Trillion by 2030?

THE NOTION THAT THE SEMICONDUCTOR INDUSTRY WILL SURPASS THE $1 Trillion mark in sales by 2030 is increasingly cited as fact… but is it realistic? It's easy to believe that it will happen, given the dizzying growth the industry has experience over the last two years, fueled of course by the pandemic, the digital transformation of the world in general (the "metaverse"), plus automotive, 5G, AI, quantum computing, VR/AR, cloud computing, Industry 4.0 and digital medicine.

In the Fall of 2021, the World Semiconductor Trade Statistics (WSTS) organization projected that the industry's worldwide sales of $553.0 billion in 2021, a 25.6% increase from the 2020 sales total of $440.4 billion. The WSTS is projecting that the industry would reach $601.5 billion in annual sales in 2022.

Another $400 billion in just eight years? At ISS, Gartner's Mark Johnson provided something of a reality check. Gartner is forecasting that the industry will reach $790 billion by 2026. Coining the term "terabuck" for $1 trillion, which Johnson said has a nice ring to it, that's about "0.8 terabuck." What will it take to get to 1 terabuck?

One red flag is the compound annual growth rate (CAGR) needed. Gartner is projecting a 9% CAGR from 2020 to 2026. Johnson said this was mainly due to huge push upward in 2020 and 2021. Underlying that was an increase in sales prices of semiconductors. "It's not necessarily a volume increase, but a price increase," he said. "That's what happens every time you start running into shortages. Prices go up. The law of supply and demand still exists and still drives the industry." Prices will go back down after supply issues stabilize, he predicts.

Getting to 1 terabuck in 2030 will require a CAGR of close to 8% over the 2020-2030 time period. "If you go back and look at when the industry has delivered a 10 year CAGR of 8%, it's once in recent history," Johnson said. "That was the period that ended at the dot.com boom, in 2000. We all know what happened after that, and it's something I don't think we would want to repeat. If you look at it from that standpoint, that sustained growth rate over a decade is really something that we haven't seen in the industry before," he said. "Anytime you start seeing these things go above the trend line, you get a little bit suspicious." More likely, we'll hit the $1T goal more in the 2031-2033 timeframe.

Other headwinds include the huge wafer fab capacity that will need to be put into place — almost double of what it was in 2020. That requires huge resources in terms of land, water and power. It also means more people: 90,000 additional workers will be required (according to an estimate during an ISS panel session), which might be the biggest challenge of all.

It's all doable, of course — it's just a question of when… and at what cost.

—Pete Singer, Editor-in-Chief

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news

Ongoing Lockdowns in China Threaten Disruptions in Global Electronics Supply Chain

Lockdowns underway in China to control the spread of COVID-19 are raising the specter of significant disruptions in the global supply chain for electronic components and consumer electronics, according to analysis by Omdia.

Major cities in China are implementing restrictive measures to halt the spread of COVID-19 under the country's "zero COVID-19" policy. In the lockdown areas, city residents are under orders to stay in their homes.

Many major manufacturers of essential electric components and car parts are located in the lockdown regions, and several factories in the regions have shut down because they are unable to recruit workers from outside the cities to keep the plants operating.

In some factories, employees have stayed and continued production. But with lockdowns continuing for extended periods, and even expanding into neighboring cities, the procurement of components to feed factory lines has been disrupted.

Logistics impacts

The lockdowns are also causing logistics issues. Truck drivers transporting products from factory to factory, or from factory to port, across city boundaries have been ordered to take daily COVID-19 tests. Drivers at risk of infection must be quarantined.

Delays in customs clearance in Shanghai and nearby ports are also causing disruptions, as are transport restrictions in Kunshan.

Despite the transportation issues caused by a shortage of truck drivers, companies can operate their factories for the time being using their inventories. But safety stocks will only be able to support plant operations for a finite period, and the impact on production will increase if the lockdowns continue for an extended period.

Polarizer supply disruption affecting iPads and MacBooks

Nitto Denko's polarizer backend process factory is located in Shanghai. Polarizers for game consoles, smartphones, and Apple MacBooks and iPads are processed in Nitto Denko's Shanghai backend process line, and they are shipped to the panel module line.

If the Shanghai lockdown continues until the end of April, the disruption of supply could impact the production of MacBooks and iPads for April.

Nitto Denko does have other backend process factories in Shenzhen and

worldnews

USA — **Semiconductor Research Corporation (SRC)** announced was selected by the **U.S. Department of Commerce's National Institute of Standards and Technology's (NIST) Advanced Manufacturing Office** to define the future technology goals of the microelectronics and advanced packaging technology (MAPT) industry.

USA — **Navitas Semiconductor** announced its membership of **PowerAmerica**, the consortium working to accelerate the adoption of next generation GaN and silicon carbide (SiC) power electronics.

ASIA — **Renesas** Donated €1 million to support humanitarian aid for Ukraine.

ASIA — **Toppan** entered into a share transfer agreement with **Majend Makcs Co., Ltd.** a manufacturer and supplier of flexible packaging headquartered in Ayutthaya, Thailand.

EUROPE — **PhotonDelta**, a cross-border ecosystem of photonic chip technology organizations, has, subject to conditions, secured €1.1 billion in public and private investment. Its goal is to "transform the Netherlands into the leader of the next generation of semiconductors."

USA — **Bechtel** announced the formation of its new Manufacturing and Technology business to address growing customer and market demands for engineering, procurement, and construction services in the semiconductor, electric vehicle, synthetic materials, and data center sectors.

NEWS & BLOGS

IPCC 6th Assessment Report Working Group III — Mitigation

A previous post from Edwards looked at the at 6th Assessment Report (AR6) from the UN's International Panel on Climate Change (IPCC). The latest contribution to the AR6, Climate Change 2022: Mitigation of Climate Change published April 4th by the panel's Working Group III, provides an updated global assessment of climate change mitigation progress and pledges, and examines the sources of global emissions.
https://bit.ly/3v0OFFu

TechInsights Takes Reverse Engineering into the Cloud

At last year's ISTFA conference, Chris Pawlowicz from TechInsights presented a paper "The Role of Cloud Computing in a Modern Reverse Engineering Workflow at the 5nm Node and Beyond." Integrated Circuit reverse engineering (RE) provides critical information to many players in the semiconductor business. Companies wanting to verify designs by taking off-the-shelf parts and recreating the electrical schematics of the original design (for competitive analysis, intellectual property infringement, security concerns, counterfeit parts, and failure analysis reasons), need their own RE capability or that of a company such as TechInsights.
https://bit.ly/3xHF6NM

Vietnam, but it would be challenging to immediately provide backup for the Shanghai facility because of limited available capacity. Notably, Shenzhen was already in lockdown for seven days in early March, and it currently is working to make up for production lost during that period.

There are plans for production in areas that are not in lockdown, but the backend process factory is located close to the panel module line to reduce logistics and other costs. For this reason, it is not easy to use other polarizer manufacturers' factories or supplies sourced from other regions.

Beyond Shanghai

Outside of Shanghai, Heungmei Optoelectronics (HMO, formerly Kunshan Chimei), the second polarizer supplier in China, has two lines located in Kunshan, mainly producing TV polarizers. However, because of the rapid spread of the COVID-19 in nearby Shanghai, the entire city of Kunshan went into lockdown from April 6.

The original plan was to lock down the city until April 12, but as the situation in its neighboring city Shanghai is getting worse, the lockdown will likely be extended to April 19, raising concerns about the production disruption of TV panels.

HMO mainly supplies polarizers for large TV panels and provides polarizers to most Chinese panel makers, including CEC-Panda, CHOT, China Star, HKC, and SIO. Since most panel makers have about two weeks of polarizer inventory, the lockdown in the Kunshan area has not immediately impeded panel production.

However, if the lockdown is longer than the original schedule, the HMO inventory held by panel makers could run out by mid-April. Moreover, HMO's inventory of subfilms is short as ports are closed. Assuming that the polarizer supply is stopped for April, the TV panel production area may decrease by over 5% in the second quarter of 2022.

Guangzhou area and Shanjin Optoelectronics

The Guangzhou area is also likely to be in lockdown, with school classes having already moved online. Shanjin Optoelectronics has a production site in Guangzhou, with two lines in operation. In addition, two lines have been relocated from South Korea to China and are preparing for mass production in 2022.

Table 1. China City Lockdown Schedule

CITY	LOCKDOWN SCHEDULE	NOTES
Shenzhen	From March 12 to March 18	China's most prominent tech hub
Shanghai	From March 28 (ongoing)	China's biggest port
Kunshan	From April 2 to April 19 (originally, it was scheduled to end on April 12)	Stopped production of electric components such as printed circuit board (PCB), connector, antenna, and polarizer.
Guangzhou	Highly likely to be the next lockdown city	Switched to online learning

If the plant shuts down because of lockdown, polarizer production from two existing lines will decrease, and the stabilization of the new line will also be more delayed than expected.

Panel makers are already turning to other polarizer makers to ensure supplies of polarizers, and they are trying to order more quantities to ensure safety inventory. Currently, panel makers are requesting Taiwan-based CMMT, Sunnypol, BQM, and Samsung SDI to increase polarizer production to compensate for the decrease in HMO production.

However, transportation restrictions are increasing supply chain risks as well as transportation costs, which could lead to a rise in the polarizer price. For a similar example, in February 2020, when the supply of polarizers was insufficient due to the lockdown policy in Wuhan, the polarizer price stopped falling, and the price of some polarizer products increased.

About the Author: Irene Heo is Omdia's Senior Principal Analyst for display materials and components research, focusing on optical films for displays and touch panels. She provides insights by covering various optical film industries and delivering market forecasts based on the panel and set markets, supply/demand and technology dynamics, pricing and cost modeling, and makers' strategies.

Top Five Leaders Continue Expanding Share of Global IC Fab Capacity

At the end of 2021, 57% of the industry's total monthly wafer capacity was owned by the top five companies. One year earlier the share was 56% and back in 2018 it was 53%. A decade ago, the share held by the top five was about 40%. The industry continues to get more top heavy regarding the composition of companies fabricating ICs. This analysis comes from Knometa's recently released Global Wafer Capacity 2022 report.

Combined, the top five companies

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had the capacity to process 12.2 million wafers per month at the end of the year, or 10% more than the year before. That growth rate was one percentage point higher than for the industry's total capacity.

Samsung — In 2021, the company widened its lead as the industry's biggest source of fab capacity. At the end of the year, Samsung held 19% of total global IC wafer capacity and 44% more capacity than the second largest company TSMC. Samsung boosted its capital spending 45% in 2020 and that translated into a sizable increase in available capacity in 2021. Most of the money was spent on the construction of multiple 300mm fab lines at its site in Pyeongtaek.

Samsung said at its 2021 Investors Forum that, when compared to its 2017 capacity level, the company's fab expansion plans will result in a tripling of capacity by 2026. Those plans will include a new $17 billion fab to be built in Taylor, Texas, the construction of which is due to start in 2022. The Taylor fab will support the company's strong push to expand foundry services for leading edge processes.

TSMC — The company's capacity growth in 2021 was relatively mild, but strong demand for its services spurred a significant increase in capital spending during the year that will result in a higher capacity growth rate in 2022. TSMC plans to remain aggressive with its spending in 2022 and 2023 as well.

Most of TSMC's recent fab construction activity has been centered at its Fab 18 site in Tainan. The company recently started adding capacity again at its Fab 12 site in Hsinchu. The last fab phase to open at the site was Phase 7 in 2017. Fab 12 Phase 8 is under construction and scheduled to begin operations in 2022.

TSMC has also experienced strong demand for mature technologies, especially for 28nm CMOS. To meet this demand, the company is expanding its Fab 16 facility in China to double the capacity there by mid-2023.

Fabs at three entirely new or "greenfield" sites around the globe are or soon will be under construction. The first phase of a large fab site (Fab 21) in Phoenix, Arizona, is already under construction and will begin processing 300mm wafers in 2024. The $12 billion Fab 21 Phase 1 plant will be used to make chips with 5nm technology. In Kumamoto, Japan, TSMC partnered with Sony to build a $7 billion 300mm fab that will also open in 2024. In November 2021, the company announced the selection of Kaohsiung as the site for another fab complex in Taiwan.

Micron — The company's capital spending the past couple years has been focused more on upgrading existing capacity for more advanced processing capabilities than on increasing capacity. Nevertheless, the company made some additional capacity available in 2021 in the form of phase 4 at Fab 15, phase 2 at Fab 16, and an expansion of its legacy products fab in Virginia.

During Micron's fiscal Q1 2022 earnings call it was reported that for both DRAM and NAND the company plans to achieve bit supply growth with node transitions through the middle of the decade. In other words, Micron's capital spending is focused on new technologies and equipment that will enable it to increase chip production volumes via die shrinks for DRAM and continued 3D scaling for 3D NAND. As a result, the company will not bring online any major fab expansions in the next couple years. The next big fab project for Micron, announced in October 2021, is the construction of a new 300mm fab at its site in Hiroshima. This fab will open for production in 2024.

SK Hynix — After boosting its capital spending substantially in 2018 for the construction of new fabs in Korea and China, SK Hynix scaled back

Global IC Wafer Capacity Leaders

(Installed Monthly 200mm-equiv. Capacity at Year-End)

2021 Rank	2020 Rank	Company	HQ Region	Dec-2020 Capacity (K w/m)	Share of Worldwide Total	Dec-2021 Capacity (K w/m)	Share of Worldwide Total
1	1	Samsung	Korea	3,364	17%	4,050	19%
2	2	TSMC	Taiwan	2,647	13%	2,803	13%
3	3	Micron	Americas	1,931	10%	2,054	10%
4	4	SK Hynix	Korea	1,881	10%	1,982	9%
5	5	Kioxia/WD	Japan	1,283	7%	1,328	6%
		TOTAL		11,104	56%	12,217	57%

©2022 Knometa Research, *Global Wafer Capacity 2022*

Includes image sensors

expenditures in 2019 and 2020. Fab M15 in Cheongju and Fab C2F in Wuxi both began operations in 2019 but ramping of capacity and production at the fabs has been gradual. The company lifted its capex significantly in 2021 and that should translate to a larger increase in capacity for 2022.

Construction of the company's newest fab, M16 in Icheon was finished in early 2021 and the company began operations in the fourth quarter of the year.

In December 2021, SK Hynix took ownership of Intel's Fab 68 facility in Dalian, China. However, the fab is still used by Intel to fabricate 3D NAND chips, so its capacity at the end of 2021 was not included as part of SK Hynix. The acquisition of Intel's NAND and SSD businesses by SK Hynix is a multiple-stage transaction over several years and stipulates that Intel can use the fab for wafer fabrication until March 2025, when SK Hynix will complete the purchase.

Kioxia/Western Digital — Capacity jointly owned by Kioxia and Western Digital increased at the lowest rate among the top five companies in 2021. The partners are increasing 3D NAND die production volumes more by 3D scaling advancements than by increasing capacity. Western Digital's President of Technology & Strategy, Srinivasan Sivaram reported in December 2021 that the company's approach to production capacity is currently about "95% conversion, 5% new wafers," meaning that nearly all its product supply needs are being met by converting to new technologies. For 3D NAND, that means increasing NAND layer counts on the chips to achieve a greater amount of memory storage per unit area. Mr. Sivaram has said Western Digital has a clear roadmap to more than 300 layers in the next four to five years.

Kioxia and Western Digital have a new fab at their site in Yokkaichi scheduled to begin operations in early 2023. Like other fabs at the site, the Y7 fab will be built in two phases. In April 2022, the partners started building a second fab at their site in Kitakami. The existing K1 fab started production in 2020 and the new K2 fab is expected to start up in 2024. sD

Worldwide Semiconductor Revenue Grew 26% in 2021

Worldwide semiconductor revenue totaled $595 billion in 2021, an increase of 26.3% from 2020, according to final results by Gartner, Inc.

"The events behind the current chip shortage continue to impact original

Table 1. Top 10 Semiconductor Vendors by Revenue, Worldwide, 2021 (Millions of U.S. Dollars)

2021 RANK	2020 RANK	VENDOR	2021 REVENUE	2021 MARKET SHARE (%)	2020 REVENUE	2020-2021 GROWTH (%)
1	2	Samsung Electronics	73,197	12.3	57,181	28.0
2	1	Intel	72,536	12.2	72,759	-0.3
3	3	SK Hynix	36,352	6.1	25,854	40.6
4	4	Micron Technology	28,624	4.8	21,780	31.4
5	5	Qualcomm	27,093	4.6	17,664	53.4
6	6	Broadcom	18,793	3.2	15,754	19.3
7	8	MediaTek	17,617	3.0	10,988	60.2
8	7	Texas Instruments	17,272	2.9	13,619	26.8
9	10	NVIDIA	16,815	2.8	10,643	58.0
10	14	AMD	16,299	2.7	9,665	68.6
		Others (outside top 10)	270,354	45.4	214,982	25.8
		TOTAL MARKET	**594,952**	**100.0**	**470,889**	**26.3**

Source: Gartner (April 2022)

equipment manufacturers (OEMs) around the world, but the 5G smartphone ramp up and a combination of strong demand and logistics/raw material price increases drove semiconductor average selling prices (ASPs) higher, contributing to significant revenue growth in 2021," said Andrew Norwood, research vice president at Gartner.

Samsung Electronics regained the top spot from Intel for the first time since 2018, though by less than a percentage point, with revenue increasing 28% in 2021 (see Table 1). Intel's revenue declined 0.3%, garnering 12.2% market share compared to 12.3% market share for Samsung. Within the top 10, AMD and Mediatek experienced the strongest growth in 2021 at 68.6% and 60.2% growth, respectively.

The most significant shift among the semiconductor vendor ranking in 2021 was HiSilicon dropping out of the top 25. "HiSilicon's revenue declined 81%, from $8.2 billion in 2020 to $1.5 billion in 2021," said Norwood. "This was a direct result of the U.S. sanctions against the company and its parent company Huawei.

"This also impacted China's share of the semiconductor market as it declined from 6.7% share in 2020 to 6.5% in 2021. South Korea had the largest increase in market share in 2021 as strong growth in the memory market propelled South Korea to garner 19.3% of the global semiconductor market."

Automotive and wireless communications segments experienced strong demand in 2021

2021 saw strong demand return to the automotive and industrial markets compared to the weak, COVID-disrupted market in 2020. The automotive market outperformed all other end markets, growing 34.9% in 2021. Wireless communications, which is dominated by smartphones, saw growth of 24.6%. The number of 5G handsets produced reached 556 million in 2021, up from 251 million units in 2020, and enterprises upgraded their Wi-Fi infrastructure for employees heading back to the office.

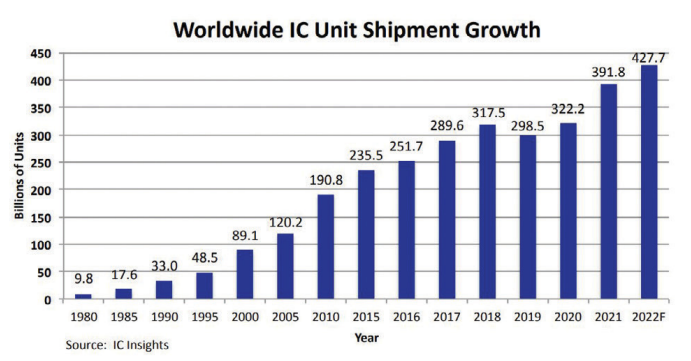
Driven by DRAM, memory accounted for 27.9% of semiconductor sales in 2021 and experienced 33.2% revenue growth, increasing $41.3 billion over the previous year. Memory continued to benefit from the key demand trend in the last couple of years — the shift to home/hybrid working and learning. This trend fueled increased server deployments by hyperscale cloud service providers to satisfy online working and entertainment, as well as a surge in end-market demand for PCs and ultramobiles.

Total IC Unit Shipments Forecast to Climb 9% This Year

IC Insights forecasts worldwide IC unit shipments will increase 9.2% this year to 427.7 billion units and resume tracking with the long-term IC unit compound annual growth rate (CAGR) of 9.4%. The 9.2% gain anticipated this year follows the large, 22% increase experienced during the economic recovery of 2021—the largest increase in IC unit growth since the boom year of 2010.

Figure 1 shows IC unit shipments in 2022 are forecast to reach a record-high level of 427.7 billion, almost 5x more units than were shipped in the year 2000 and nearly 44x more than were shipped in 1980.

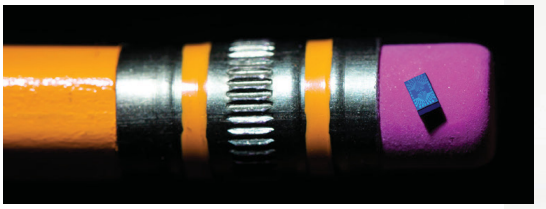
The figure shows there was a falloff in shipments in 2019, which was only the fifth time in the history of the IC market that there was a year-over-year decline in IC unit volume. The previous four years with a drop in units were 1985, 2001, 2009, and 2012. Never have there been two consecutive years with a decline in IC unit shipments.

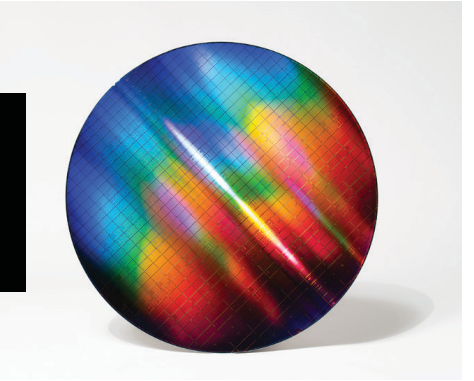


Of the 33 major IC product categories defined by the World Semiconductor Trade Statistics (WSTS) organization, 30 are forecast to show positive unit growth in 2022 and three (SRAM, DSP, and Gate Array) are forecast to have unit shipment declines. Twelve product segments are forecast to match or grow more than the expected 9.2% growth rate for total IC units this year.

From 2021-2026, IC Insights forecasts the IC unit CAGR will be 7%. Ignoring the 5-year CAGR time periods with abnormally high or low endpoints, IC Insights believes that the long-term CAGR for IC unit growth will be 7%-8%, moderately lower than the historical 42-year rate of 9.4%.

Intel and QuTech Collaborate to Produce Silicon Qubits at Scale





Researchers at Intel and QuTech, an advanced quantum computing research center consisting of the Delft University of Technology (TU Delft) and the Netherlands Organization for Applied Scientific Research (TNO), have successfully created the first silicon qubits at scale at Intel's D1 manufacturing factory in Hillsboro, Oregon. The result is a process that can fabricate more than 10,000 arrays with several silicon-spin qubits on a single wafer with greater than 95% yield. This achievement is dramatically higher in both qubit count and yield than the typical university and laboratory processes used today.

This research was published in the journal Nature Electronics and is Intel's first peer-reviewed research demonstrating the successful fabrication of qubits on 300mm silicon. The new process uses advanced transistor fabrication techniques including all-optical lithography to produce silicon-spin qubits, the same equipment used to produce Intel's latest-generation complementary metal-oxide-semiconductor (CMOS) chips. The groundbreaking research is a crucial step forward in the path toward scaling quantum chips, demonstrating that it's possible for qubits to eventually be produced alongside conventional chips in the same industrial manufacturing facilities.

"Quantum computing has the potential to deliver exponential performance for certain applications in the high-performance compute space," said James Clarke, director of Quantum Hardware at Intel. "Our research proves that a full-scale quantum computer is not only achievable but also could be produced in a present-day chip factory. We look forward to continuing to work with QuTech to apply our expertise in silicon fabrication to unlock the full potential of quantum." SD

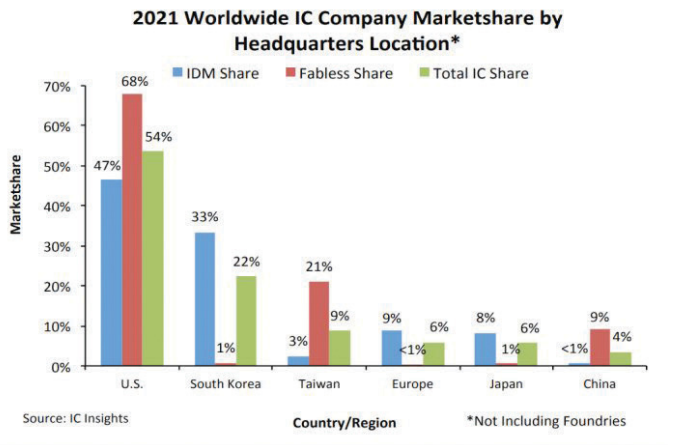
Chinese Companies Hold Only 4% of Global IC Market Share

U.S. companies captured 54% of the total worldwide IC market in 2021, propelled by a 47% share of IDM sales and a 68% share of fabless sales.

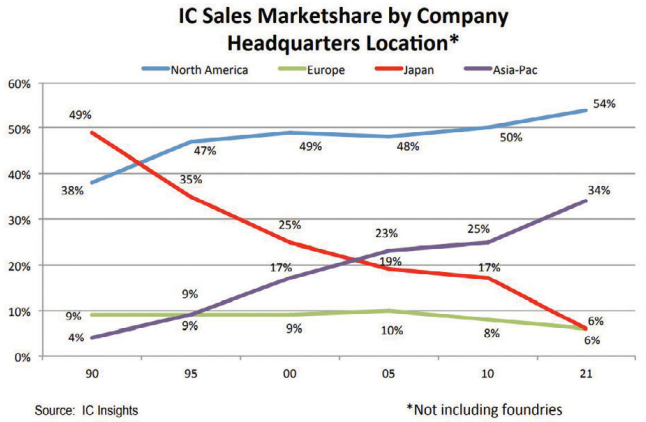
Regional market shares of IDMs (companies with wafer fabs), fabless companies, and total IC sales were led by U.S. headquartered companies in 2021, according to the 2Q Update to The McClean Report 2022 that will be released in May.

Figure 1 shows the 2021 IDM and fabless company shares of IC sales as well as the total worldwide share of the IC market by company headquarters location (pure-play foundries are excluded from this data).

U.S. companies held 54% of the total worldwide IC market (the combined total of IDM and fabless IC sales) in 2021 followed by the South Korean companies with a 22% share. Taiwanese companies, on the strength of their fabless company IC sales, held 9% of global IC sales as compared to a 6% share held by the European and Japanese suppliers (the Taiwanese companies first surpassed the European companies in IC industry market share in 2020).



The South Korean and Japanese companies have an extremely weak presence in the fabless IC segment and the Taiwanese and Chinese companies have a very low share of the IDM portion of the IC market. Overall, U.S.-headquartered companies show the most balance with regard to IDM, fabless, and total IC industry market share.



In 2021, the Japanese companies' IC sales market share continued its decent that first began in the 1990s. As shown in Figure 2, Japanese companies held almost half of the worldwide IC market share in 1990 only to see that share fall precipitously over the past 30 years to only 6% in 2021. While the European companies' market share decline has not been as steep as the Japanese companies, the European firms also held only a 6% share of the global IC market last year, down from 9% in 1990.

In contrast to the Japanese and European companies' IC market share slide over the past three decades, the U.S. and Asian IC suppliers have seen their shares climb since 1990. As shown in Figure 2, the Asian companies have witnessed their share of the worldwide IC market surge from a miniscule 4% in 1990 to 34% in 2021. This increase in share by the Asian IC suppliers equates to a 31-year IC sales CAGR of 15.9%, almost double the total IC market CAGR of 8.2% over this same time period.

2021 Global Semiconductor Equipment Sales Surge 44% to Industry Record $102.6 Billion

Worldwide sales of semiconductor manufacturing equipment in 2021 surged 44% to an all-time record of $102.6 billion from $71.2 billion in 2020, SEMI, the industry association representing the global electronics product design and manufacturing supply chain, reported. The data is now available in the Worldwide Semiconductor Equipment Market Statistics (WWSEMS) Report.

China claimed the largest market for semiconductor equipment for the second time with sales expanding 58% to $29.6 billion to mark the fourth consecutive year of growth. Korea, the second-largest equipment market, registered a sales increase of 55% to $25.0 billion, after showing strong growth in 2020. Taiwan logged 45% growth to $24.9 billion to claim the third position. Annual semiconductor equipment spending increased 23% in Europe and 17% in North America, which continues to recover from a contraction in 2020. Sales in Rest of the World jumped 79% in 2021.

"The 44% increase in manufacturing equipment spending in 2021 highlights the global semiconductor industry's aggressive push to add capacity," said Ajit Manocha, SEMI president and CEO. "This drive to expand production capabilities extends beyond the current supply imbalance, as the industry continues to ramp up to address a wide range of emerging high-tech applications that will enable a smarter digital world with countless social benefits."

Annual Billings by Region in Billions of U.S. Dollars with Year-Over-Year Change Rates

REGION	2021	2020	% CHANGE
China	29.62	18.72	58%
Korea	24.98	16.08	55%
Taiwan	24.94	17.15	45%
Japan	7.80	7.58	3%
North America	7.61	6.53	17%
Rest of the World	4.44	2.48	79%
Europe	3.25	2.64	23%
Total	**102.64**	**71.19**	**44%**

Source: SEMI (www.semi.org) and SEAJ (www.seaj.or.jp), April 2022

Global sales of wafer processing equipment rose 44% in 2021, while other front-end segment sales grew 22%. Assembly and packaging showed exceptional growth across all regions, resulting in an 87% market increase in 2021, while total test equipment sales rose 30%.

Compiled from data submitted by members of SEMI and the Semiconductor Equipment Association of Japan (SEAJ), the Worldwide SEMS Report is a summary of the monthly billings figures for the global semiconductor equipment industry. Equipment categories cover wafer processing, assembly and packaging, test, and other front-end equipment including mask/reticle manufacturing, wafer manufacturing, and fab facilities.

Continued on page 30

Sub-fab Improvements Require Reliable Real-time and High Sensitivity In-situ Data

MARTIN MASON, VP Product Marketing, Atonarp

Robust, high speed and high sensitivity real-time data monitoring is essential for enabling rapid response and tight feedback loops.

THE SUB-FAB COMPONENT OF SEMICONDUCTOR FABRICATION has for decades been somewhat of a secondary afterthought. And, unlike in the bright, glistening processing corridors of the main fab, sub-fab equipment is generally conceptually relegated to lower-level systems associated with basic tool management and waste handling tasks. However sub-fab applications have been seeing a resurgence as increased vacuum intensity and control along with new safety requirements from advanced process chemistry and related safety, abatement and sustainability are driving a larger share [1] (**FIGURE 1**) of an already surging semiconductor equipment market.

The key components of a sub-fab include the dry vacuum pumps, combustion and absorber abatement systems, water handling equipment and chillers, as well as bulk materials delivery and management. As today's fabs become more complex, the lowly sub-fab comes to the fore as an increasingly more valuable component of the overall system. Sales of products used in the sub-fab area totaled around $2 billion in 2018 [1], but have been growing above the overall WFE (wafer FAB equipment) growth rates in the years since even as the the WFE market size has grown dramatically.

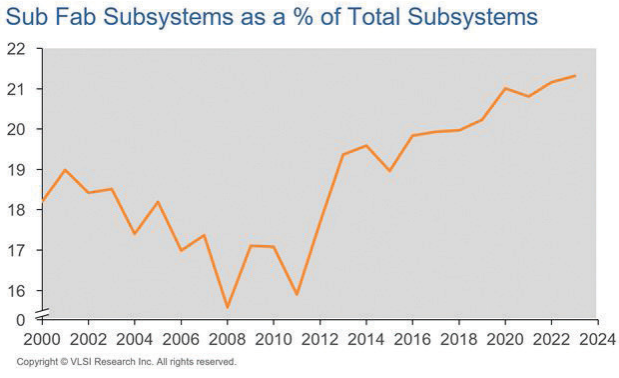


Figure 1. Sub-fab applications have been seeing a resurgence as increased vacuum intensity and control along with new safety requirements are driving a larger share. Source: VLSI Research.

However, as clients' demands for greater sustainability drive fab operators to place an increasing importance on the impact that semiconductor manufacturing has on the environment, the once-overlooked sub-fab is now seen as a critical element for reducing the fab's environmental footprint and increasing overall efficiency. Combined with increasingly stringent safety requirements, the growing importance being placed on sustainability and efficiency is giving rise to a greater focus on running sub-fab equipment smarter, with real-time in-situ monitoring and control.

Sub-fab managers have three main resources they need to manage: energy (electricity and natural gas), water and materials. By far the biggest challenge is materials management from both safety and sustainability. Green energy sources and carbon offsets are common, and water recovery and recycling are well understood and managed, however reduction and management of materials is very challenging and an area where the both the safety and sustainability issues are growing. Of course, to avoid costly downtime of the fab, the modern sub-fab must also meet the highest

reliability standards and find solutions for safety and sustainability while dealing with the constant pressure for managing costs.

The Challenge

The three fundamental pillars of sub-fab management are safety, sustainability and savings. These pillars are today receiving renewed attention:

Molecular level safety monitoring: Advanced, state-of-the-art, leading-edge logic, foundry and memory processes are using new, hazardous materials and by-products, and thus placing increasing demands in fab safety. This is particularly true in situations where selective processing chemistry is used, namely in atomic layer deposition (ALD) and atomic layer etching (ALE). A 2019 study highlighted that in the period between 2017 and 2019, more than 30 adverse events such as explosions, fires, exothermic reactions, chemical reactions and off-gassings occurred in the sub-fab area along the exhaust handling pathway leading from the chamber through the abatement systems.

Current emerging process examples where molecular safety monitoring is being implemented to great effect include high-K zirconium-based dielectric materials that are used for logic gates and DRAM capacitor constructs, where explosive metallic zirconium particles comprise a potential by-product. Additionally, high order silane (SiH_4) chemistry, which is used in the atomic level deposition of silicon oxides in flash memory manufacturing, presents challenges with regards to oxygen exposure and active molecular level leak detection for fire prevention. Hydrazine (N_2H_4), also known as rocket fuel, is finding uses in new process chemistries and unstable ammonium nitrate is a common by-product safety challenge for silicon nitride deposition using ammonia based reactant gases. The detection of other hazardous by-product gases and 'gunk' condensates must be carefully monitored and managed to prevent the build-up of hazardous materials and allow for timely preventative maintenance cleans.

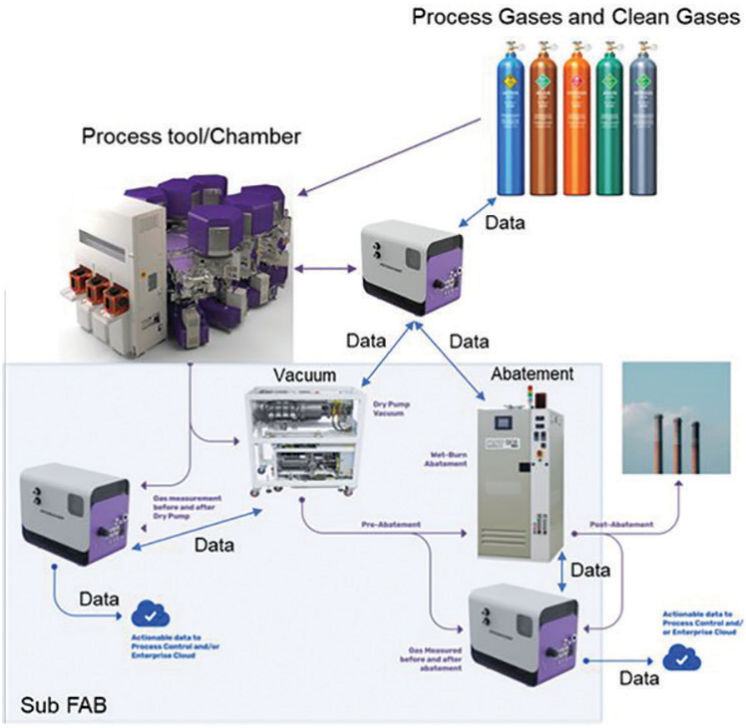


Figure 2. On chamber and in sub-fab solution from Aston that enables reliable safety and sustainability monitoring and control.

Sustainability is coming into sharp focus: A recent report from Apple [2] shows that more than 80% of a smartphone's lifetime carbon footprint including operation, is generated during the actual manufacturing process, with semiconductors contributing the largest and growing share of the total, i.e. approximately 40%.

While green energy use and water recycling efforts recently implemented in fabs have made a major impact on greenhouse gas emission and water consumption metrics, the material portion of the semiconductor fab sustainability challenge continues to grow as a percentage of the total.

Identifying a robust method for monitoring and reducing the overall amount of material used in the manufacturing process is a critical task for the semiconductor industry – a task that requires a highly innovative approach to in-situ materials monitoring (mass flow, consumption and waste) and requires, molecular level chemistry specific quantification. The essential first step is establishing a "baseline" for processes and equipment, which will enable changes in material use to be accurately monitored and quantified over time.

Savings derived from safety and sustainability initiatives: It goes without saying that the cost of safety equipment deployment is relatively insignificant compared to staff, equipment, production and reputation costs resulting from errors and accidents.

Sustainability initiatives deliver a more complex return-on-investment profile. Reduced material usage leads to less waste and significant reductions in associated materials and abatement related costs.

Beyond the pure cost recovery factors associated with running fabs more efficiently, many semiconductor consumers are increasingly factoring in sustainability as another component of their supplier selection criteria profile. For example, the largest consumer of semiconductors in the world, Apple, is a leader in incentivizing semiconductor fabs to reduce, reuse and recycle materials and holds them accountable for long term sustainability gains. Apple has committed itself to requiring its entire supply chain to be 100% carbon neutral

by the year 2030 [3]. Substantial and lucrative supplier contracts are commonly accompanied by fab sustainability targets – and, unsurprisingly, most of this relates to processes at the sub-fab level, where the actual waste is managed.

Further, an Edwards tool [4] that helps calculates the cost of sub-fab equipment failure and resultant unscheduled maintenance and line-yield loss, can rapidly top $20K per incident. Many failures can be anticipated with suitable equipment monitoring including molecular level materials flow through the fore-line and sub-fab dry pumps. These preventative maintenance optimization benefits are in addition to the safety and sustainability benefits.

The Solution

The common thread tying the sub-fab pillars of safety, sustainability and savings together is that, in order to improve them, one must accurately measure and quantify at high speed the managed materials and waste. There is a significant need for robust, quantified and real-time metrology both for the process chamber as well as increasingly for the sub-fab infrastructure.

The Aston family of real-time semiconductor metrology solutions from Atonarp (**FIGURE 2**) were designed from the ground up to support fabrication. Aston's best in class speed with sensitivity, at <9 ppb √Hz is up to 10x better than alternative legacy gas analysis solutions, and unlike optical emission spectroscopy, Aston requires no local plasma source, typically abscent in sub-fab and ALD/ALE processes. Aston is a compact mass spectrometer that combines high accuracy with production-ready robustness. It provides data that is immediately actionable, enabling corrective steps to be taken quickly if and when any problems are identified.

For semiconductor manufacturing, gas analyzers need to be robust enough to work with the harsh process gas chemistry, high temperature gases and by-products that are present. Aston is built to reliably and repeatedly handle such conditions, which is something that cannot be said for other solutions commonly used in the industry.

When compared to standard residual gas analyzers possessing the appropriate level of robustness, Aston achieves results that are 3x to 10x better for the key sensitivity/speed metric. This superior performance enables Aston to improve safety and sustainability in advanced sub-fab applications, whilst significantly reducing costs at the same time.

Summary

The oft-overlooked sub-fab will, of course, continue to get somewhat less attention than the glistening semiconductor fab, but it is becoming increasingly recognized as a substantial contributing factor to the overall sustainability, safety and cost reduction mix.

In order to achieve the necessary improvements at the sub-fab level, robust, high speed and high sensitivity real-time data monitoring is essential for enabling rapid response and tight feedback loops. Atonarp's Aston is an exceptionally reliable, flexible gas analyzer that provides the data needed for the achievement of noticeable improvements to the sub-fab … and to the bottom line. sD

REFERENCES

1. https://www.semi.org/en/blogs/business-markets/critical-subsystems-in-the-sub-fab
2. Product Environmental Report. iPhone 13 Sep. 14, 2021. Apple Inc.
3. https://www.apple.com/uk/newsroom/2020/07/apple-commits-to-be-100-percent-carbon-neutral-for-its-supply-chain-and-products-by-2030/
4. https://www.edwardsinnovation.com/operational-excellence/value-calculator/?utm_campaign=Operational%20Excellence&utm_source=SQDCEP%20E-Book&utm_medium=Cost&utm_content=SubFab%20Value%20Calculator

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Intel 'Has a Shot' at Performance Leadership

DAVID LAMMERS and **PETE SINGER**, Semiconductor Digest

Getting EUV tools may be challenging.

WHEN INTEL CEO PAT GELSINGER announced in July of last year that Intel intended to roll out four transistor technology generations in five years, achieving performance-per-Watt parity with the leading foundries in 2024 and leadership in 2025, many scoffed. How could the company that had gone from unchallenged leader to struggling follower, the sceptics argued, make such a transformation?

However, leaders of Intel's Logic Technology Development (LTD) organization recently have affirmed that Intel is meeting its development benchmarks for the 4nm, 3nm, 20Å (Angstrom), and 18Å nodes. Moreover, Sanjay Natarajan, LTD's co-general manager, said Intel would be ready with its 18Å node by the end of 2024, one quarter earlier than previously announced.

D1X Mod 3 provides 270k sq. ft. of clean room. *(Source: Intel)*

In a press briefing, Natarajan said Intel benchmarks its progress in detail. "Indicators for all of these technology nodes are all very positive," he said. "We are on or ahead of our milestones for each of them."

As the Intel managers were speaking to reporters, Scotten Jones, an industry analyst who closely follows the progress of Intel and foundries TSMC and Samsung in logic technology, was presenting at the SEMI Industry

Strategy Symposium (ISS). After detailing Intel's failures during the 14nm and 10nm nodes, Jones said there are indicators Intel is keeping on schedule with its "Intel Accelerated" plans.

"I think Intel really does seem to have made a big turnaround in their ability to develop and introduce these technologies," Jones said. "If they execute on this accelerated roadmap, which they appear to be doing, they could be the performance leader in 2025. I think TSMC might still be the density leader, while Intel could be the performance leader. Intel is claiming they'll be a performance leader in 2025. I think they have a good shot of doing that."

Jones, who runs a consultancy, IC Knowledge LLC (Georgetown, Mass.), focused on modeling semiconductor costs, noted that performance is Intel's primary concern for its microprocessor products, while TSMC puts more emphasis on density and power. Starting at the 20Å node, Intel plans to introduce its version of the Gate All Around transistor architecture, RibbonFET, as well as a power delivery architecture on the backside of the wafer, called PowerVia. Jones said by putting four thick metal layers on the underside, it may help solve the IR drop challenges which are so critical for high-performance devices.

High NA EUV at Intel

EUV's successful development by ASML and its lithography ecosystem partners is largely responsible for the Moore's Law advances over the past few years. Ironically, while Intel strongly supported EUV's development, the company hesitated to bring EUV scanners into production as soon as its leading competitors. Jones said "Samsung and TSMC have really broken the ground on EUV. There's been a lot of learning, some of which was about how to keep those tools productive. And Intel's going to benefit from all that. It's going to make it a little easier for them."

Intel plans to be the first commercial customer of the High N.A. (numerical aperture) scanner being developed by ASML. Natarajan said Intel's plan is to be "first to high N.A." in 2025. However, he added that "our strategy is to be incredibly flexible. If the (high N.A. EUV) tools come in and we are mature and ready," including the EUV ecosystem of resists, pellicles, and more advanced mask writers, then Intel will use the high N.A. tools "in that 2025 time frame. We also have contingencies; if high NA is not ready, we have a .33 N.A. solution for those layers. We will be able to play it both ways."

With Intel engaging with external customers as part of the Intel Foundry initiative, Natarajan said Intel is communicating to internal and external customers about its contingency plans in case the high N.A. solution is not ready until 2026. "We will not be surprised either way. We know that this involves a huge amount of ecosystem heavy lifting, not just by ASML and by Intel. How you set up the design rules, with the constraints on those layers, will be doable on .33 or .55, so that you don't box yourself in."

Ryan Russell, the co-general manager of the Logic Technology Development organization, said the Mod 3 expansion of the former Ronler Acres D1X fab (the 450-acre Ronler Acres site was renamed Gordon Moore Park at Ronler Acres) was designed to accommodate the additional height and weight of the ASML High N.A. EUV tools. The expansion adds 270k sq. ft. of clean room space to the development fab.

Russell reminded the reporters that the LTD organization came up with strained silicon, high-k metal gate, and FinFET, all well before its competitors. "All those innovations were led by Intel and came out of this facility. They propelled the industry forward. In the Angstrom era, with RibbonFET and PowerVia, we expect Intel to lead the next major transistor architecture innovations."

The PowerVia module is being developed independently, using a FinFET transistor during early development. Natarajan said back in the mid-90s Intel used to combine all of its innovations on one node, partly in order to get it all done in two years. But that forced the development team to de-bug several changes simultaneously.

With RibbonFET and PowerVia being two major changes at the 20A node, Intel decided to decouple them so the developers can learn in parallel and debug them separately. "That is a big deviation from what we might have done in the past. We are developing PowerVia on a very mature FinFET transistor so that we are not screened by transistor problems. And this way gives us visibility earlier, so we can keep to our schedule," he said.

The decoupling strategy during development, with PowerVia "bolted on" to the RibbonFET transistor later, gives the company "a little bit of contingency in case we need it."

The Mod3 expansion of the D1X fab also provides the ability to run more test wafers. CEO Gelsinger quickly approved a request for additional funding for the LTD group, including hiring more engineers, buying more advanced tools, and running more test silicon in parallel.

Gelsinger's first question to the LTD team, Russell said, was "'What do you need to accelerate Intel's process roadmap?' We put together a plan for $1.5 billion of extra engineers, tools, and silicon, and he said 'Go do it.'"

Jones said Intel's delays at the 14nm and 10nm node came in part because the company's CEO at the time was more concerned about immediate financial results than keeping the engineering team intact. After layoffs were announced, talented engineers who knew they could easily find new jobs left Intel. Jones also argued that as the process node transitions dragged, the Copy Exact strategy meant that Intel fabs were being Continued on page 20

Enhancing Performance, Quality and Yield in Current and Emerging Display Technologies

DAVID AKERSON, Sr. Global Marketing Manager, Thermo Fisher Scientific

Process metrology, failure analysis, and core-structure characterization can be invaluable in accelerating research and development, enhancing yield and improving display quality.

THE PHRASE "INFORMATION DISPLAY TECHnology" applies to a broad spectrum of devices. From smartwatches to foldable phones, interactive screens in automobiles to outdoor digital signage and billboards in cities and stadiums around the word, display technology is ever present in our lives.

Across multiple industry sectors, applications and form factors are providing new opportunities and challenges for display manufacturers (**FIGURE 1**). Opportunities include an expanding array of new use cases for display technologies, while challenges include enhancing current technologies to deliver ever-better picture quality: resolution, refresh rate, color gamut, luminance, contrast ratio, and developing the next generation of display technology. As display technologies move forward, achieving next-generation performance will require innovation in areas such as backplane technology and light-conversion efficiency.

Within the display industry, the path forward passes through mainstream, future and exploratory technologies. Today's mainstream is populated with liquid-crystal display (LCD) and active matrix organic light-emitting diode (AMOLED) technologies with many applications transitioning from LCD to AMOLED. To compete with the image quality of AMOLED, many LCD manufacturers have developed quantum-dot LED (QLED) and mini-LED. Micro-OLED displays have been developed for niche applications such as virtual reality and augmented reality. Looking to the future, display manufacturers are making investments

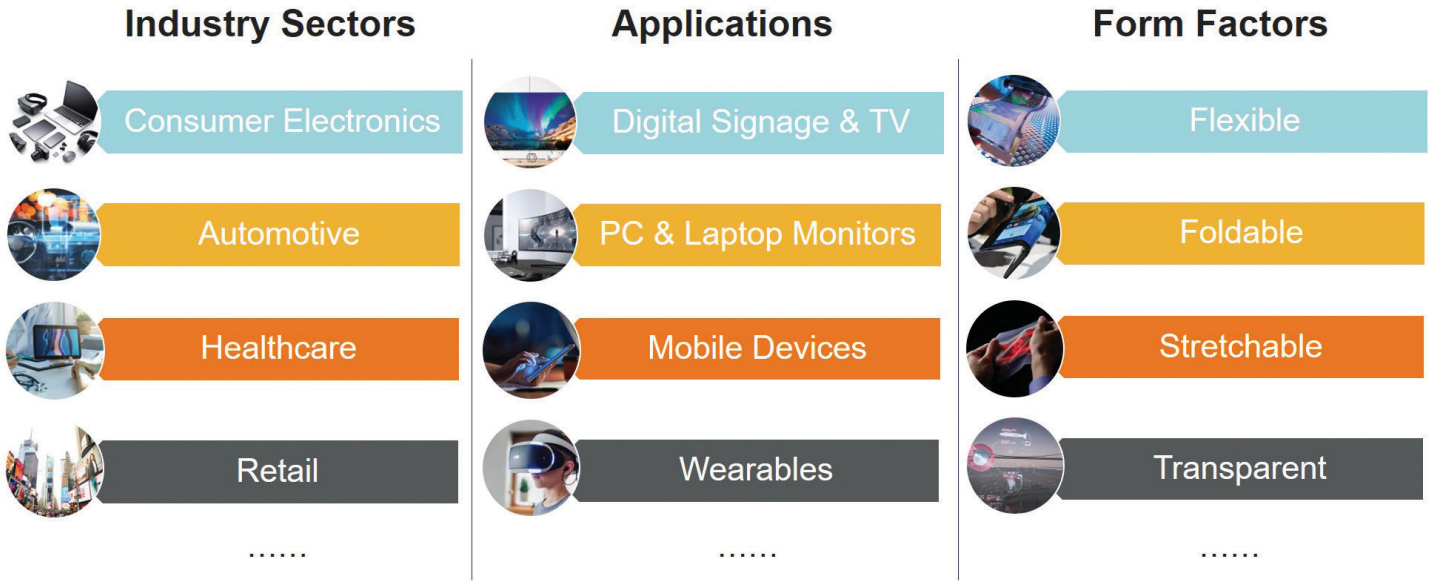


Figure 1. This marketspace model is the tip of the opportunity iceberg for display makers.

in technologies such as Red-Green-Blue (RGB) chip micro-LED and electroluminescent QLED to take displays to the next level.

For maturing and future display technologies, process metrology, failure analysis, and core-structure characterization can be the keys to accelerating research and development, enhancing yield and improving display quality. In this article, we will use a mobile device as an example to explore the challenges related to the display layers and the role process metrology, failure analysis, and core-structure characterization can play in addressing these challenges.

Understanding the display

To better understand process metrology and failure analysis challenges, it's important to have a base understanding of the display layers. In a mobile device, the display consists of three layers: the cover glass, the touchscreen and the display panel. Of the three, the display panel is the core component and consists of the thin film encapsulation (TFE) layer, the thin-film transistor (TFT) backplane and the flex substrate. **FIGURE 2** provides an example diagram of a mobile device and the layers described above and will be referred to throughout this article.

Process Metrology: Examining the Crucial Layers of Display Technology

For display manufacturers, process metrology that provides reliable and repeatable measurements is an increasingly valuable tool in identifying design and manufacturing process improvements.

Referring to the example display stack in Fig. 2, process metrology often focuses on two parts: TFT backplanes and RGB light-emitting units. In an OLED display, this can be challenging as the light-emitting units reside within the TFT backplane and are comprised of molecular layers 100 to 200 nanometers thick. In this core display technology, optical properties are the key area of interest. The surrounding TFT backplane contains inorganic layers totaling 1 to 5 microns in thickness. Crucial failures can occur here, and electrical properties are of primary interest here.

Imaging the TFT backplane

For display manufacturers, it is increasingly important to control both the lateral and vertical critical dimensions (CDs) in the TFT backplane. While measuring lateral CDs is relatively straightforward, measuring vertical CDs can be challenging.

Measuring lateral CDs is accomplished utilizing a scanning electron microscope (SEM), such as a Thermo Scientific™ Apreo 2, to provide imaging modes that highlight surface features under different contrast settings. The resolution of the imaging tool is an important factor for measuring lateral CDs.

Measuring vertical CDs is more challenging as backplane manufacturing involves thin-film deposition at the atomic level. Obtaining accurate measurements requires a focused ion beam (FIB), such as a Thermo Scientific Helios 5 FX Small DualBeam, to prepare the sample by performing a site-specific cross-cut and then applying a fine polish. The cross-section sample is then viewed with a high-resolution SEM (**FIGURE 3**).

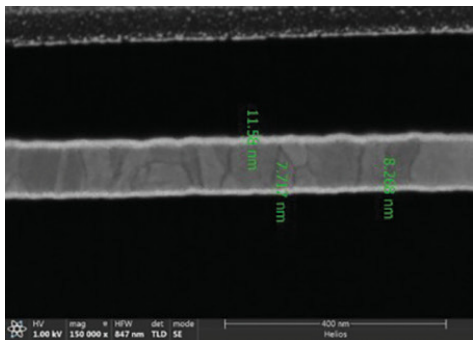


Figure 3. Viewing a TFT backplane and measuring the individual layers thickness.

Resolving the organic layers in light-emitting units

As noted above, process metrology is more challenging in light-emitting units that have features and layers at nanometer scale. OLED brings additional challenges as organic materials are low contrast under microscopic view, and also sensitive to moisture and oxygen, such that they may quickly degrade when exposed to air.

For measuring the OLED stack, there are two methods that are commonly used. The first uses FIB dual-beam sample prep combined with transmission electron microscopy (TEM) analysis. The second uses only a FIB dual-beam. For both methods, the key to success is the ability to control a sample's quality thickness and surface condition.

For TEM analysis, preparation of thin samples must cause only minimal damage to provide accurate metrology

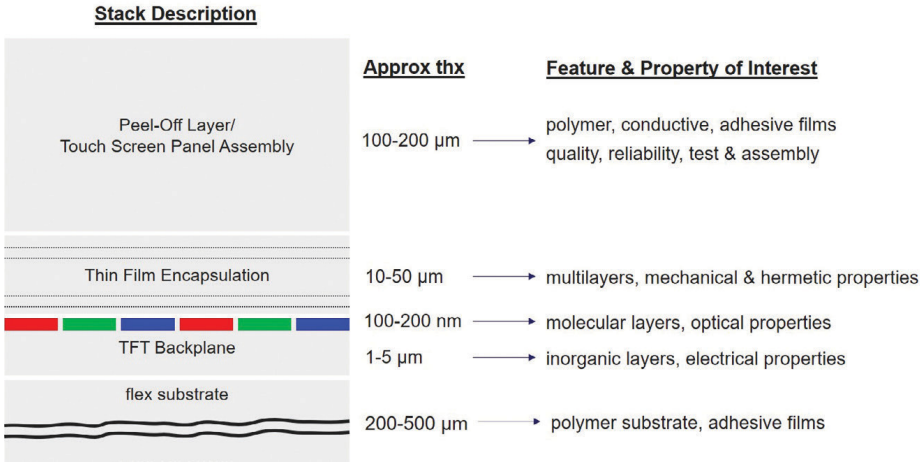


Figure 2. This example diagram of a mobile display illustrates the layers of interest that affect yield and quality.

measurements. As a result, it is important to use a FIB dual-beam with extraordinary low-kV performance. With the FIB dual-beam to TEM method, it is recommended users utilize software-based automation to ensure sample repeatability by controlling processes such as lift out and sample thinning. Once a sample has been processed to the desired thickness, it is transferred to a TEM for viewing and measurement. The benefit of this method is the TEM provides higher kV to resolve the layers. However, the risk with this method is the sample's exposure to moisture and oxygen.

In the second approach, using a FIB dual-beam only keeps the sample in vacuum during the transfer onto the in-chamber scanning/transmission electron microscopy (S/TEM) rod, preventing the degradation that results from exposure to air. Performing S/TEM analysis at 30 kV is used to highlight the contrast of organic layers (**FIGURE 4**).

Failure Analysis: Going Beyond the Limits of Optical Microscopy Workflows

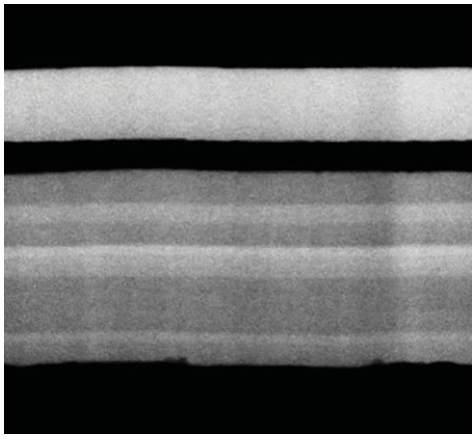


Figure 4. Using dual-beam alone, 30 kV S/TEM can resolve more than 10 layers of an OLED stack.

No matter how well-controlled or well-measured a process may be, failures will happen. Within the complex, multi-stage manufacturing process, failure analysis can be used to improve quality and yield. However, identifying failures can be challenging.

Identifying particle contamination is one example that can be especially problematic. As display resolution increases, failures can be caused by particles that are too small to detect with typical optical microscopy workflows. Also, the increasing complexity of display technology is more likely to bury unwanted particles deep inside the structure, obscuring them from optical view. For display manufacturers, the most likely victims of particle contamination are the peel-off layer, the touch screen assembly, the TFT backplane, and the flex subtrate (Fig. 2).

Finding the root causes of backplane particles

Finding backplane particles can be accomplished using a high-resolution SEM (**FIGURE 5**). It is suggested that manufacturers use a SEM along with X-ray energy-dispersive spectroscopy (XEDS) analysis to acquire elemental information about material composition. This information can help failure analysts isolate the root causes of unwanted particles and then identify ways to reduce their occurrence.

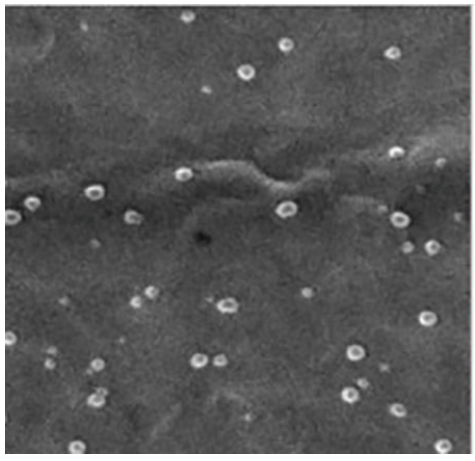


Figure 5. Unwanted backplane particles are clearly visible in this image.

Isolating and analyzing panel defects

As more architectural elements are built onto the backplane, unwanted particles can create panel defects causing dead pixels and other potentially fatal flaws. Due to the growing complexity of the display, it is important to isolate and analyze panel defects. This can be accomplished using an electrical failure analysis (EFA) workflow that proceeds from coarse to fine localization.

This workflow starts with using a lock-in thermography (LIT) system such as the Thermo Scientific ELITE™, to detect the temperature variations from electrical faults with precision on the order of a few micrometers.

The next step is to more precisely locate defects by running electrical tests on the TFT backplane. Here, the challenge lies in carefully removing just enough material to expose the underlying circuitry. This has typically been done using chemical etching; however, this approach is not site-specific and can potentially damage the circuit of interest. In this workflow example, a Thermo Scientific Helios 5 Plasma Focused Ion Beam (PFIB) SEM was used to apply gas-enhanced etching to homogeneously remove material above the circuit, expose the metal, and prepare the surface for electrical testing (**FIGURE 6**).

Electrical probing is then used to pinpoint the locations of panel defects. Depending on the size of the features, this could entail micro-probing with optical microscopy or nano-probing using the SEM.

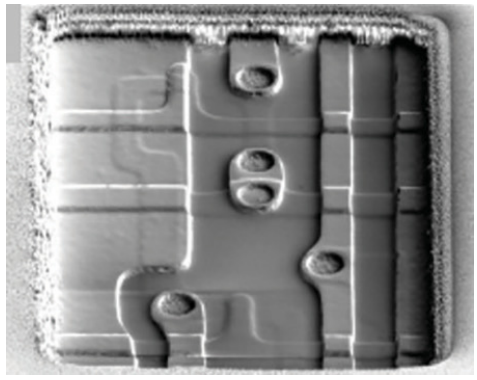


Figure 6. Precise delayering enables accurate probing and informative electrical testing of embedded circuits.

The sample can then be moved to a FIB dual-beam for cross-sectional "slice and view" visualization and analysis of the region around the defect (**FIGURE 7**). For especially small defects that require comprehensive analysis, a FIB dual-beam can be used to prepare thin samples for visualization using a TEM, such as a Thermo Scientific Talos™ F200E.

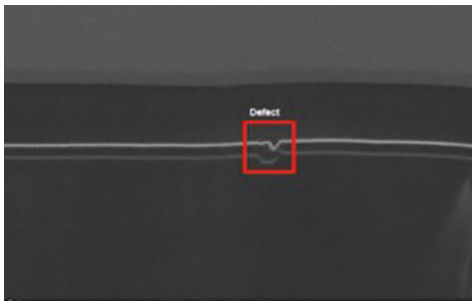


Figure 7. Slice-and-view visualization enables the precise location and analysis of defects in display panels.

Milling and imaging of multi-layer display modules

In display modules, other parts of the packaging are attached to the panel: the touchscreen assembly, the peel-off layer, and connections to driver ICs and flexible PCBs. Successful EFA of multi-layer display modules can be done utilizing a workflow similar to the one above, but in this case uses a PFIB rather than a dual-beam to accurately locate defects through many types of packaging materials.

For this application, a LIT is used to identify hotspots in touch-panel sensors, flexible PCBs, bumping areas, or driver ICs. Next, each defect is accessed and analyzed. Rather than deconstructing the packaged module, a PFIB is used to mill through different materials for full-stack cross-sectional analysis spanning large areas (**FIGURE 8**). For display modules, a PFIB is the most reliable and straightforward way to perform direct and detailed physical failure analysis (PFA).

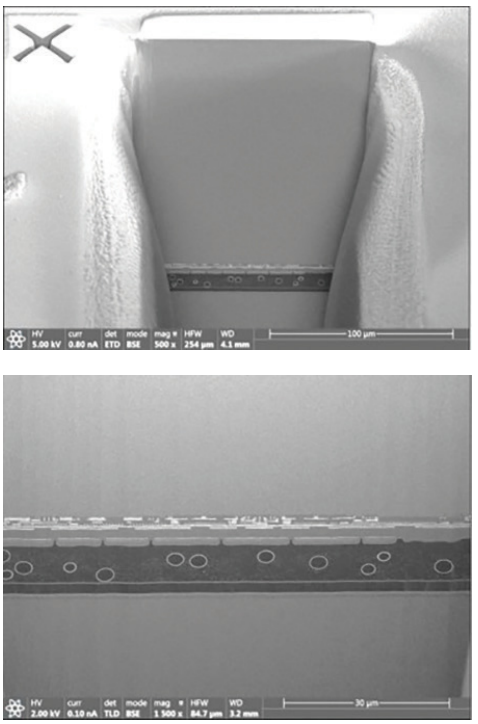


Figure 8. After precise milling with a PFIB (top), high-resolution imaging is used to analyze individual layers such as anisotropic conductive adhesives (bottom).

Materials Engineering: Solving New Challenges on the Technology Roadmap

As displays move towards next generation technologies such as micro-LED and electroluminescent QDs, which demand extreme precision in design and production, manufacturers are investigating new organic materials to extend device lifetime and improve image quality. The following are examples of challenges facing research and development efforts and how characterization tools can provide insights to accelerate development.

Encapsulating OLED layers

Because organic materials are susceptible to environmental degradation, innovation is occurring in TFE as a way to protect OLED devices, extend device lifetime and expand the range of possible applications in new form factors.

As an example, a suitable film can be created by laminating materials such as alumina (Al_2O_3) and zirconia (ZrO_2) in alternating layers. When implemented correctly, the interfaces enable the hermetic properties of OLED thin-film encapsulation, preventing the diffusion of oxygen and moisture into the OLED (**FIGURE 9**). However, it is crucial to control the thickness of every layer and identify the phase at each interface.

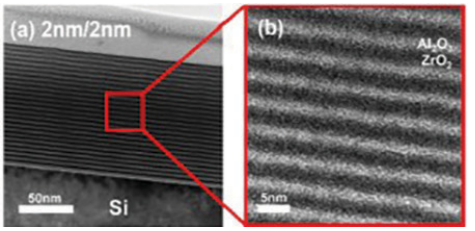


Figure 9. TEM image of alternating oxide layers. (Image from dx.doi.org/10.1016/j.tsf.2015.12.044)

When assessing these layers, a workflow that uses a dual-beam for sample preparation and a TEM for imaging provides deeper insight is recommended. In addition, high-efficiency XEDS can be utilized to acquire chemical information about the layers.

Actualizing nano-encapsulation of quantum dots

Developers of quantum dot (QD) technology are pursuing three major goals: engineering new QD types that improve image quality and extend the lifetime; exploring environmentally friendly materials; and developing technologies that actualize nano-encapsulation of nanoparticles.

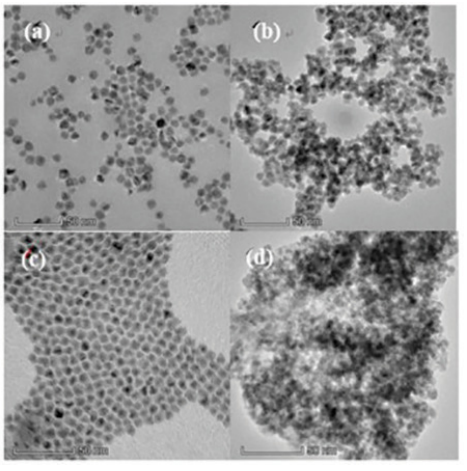


Figure 10. Analyzing particle size and distribution in QD displays. (Image from SID 2019 Digest, pages 30-33)

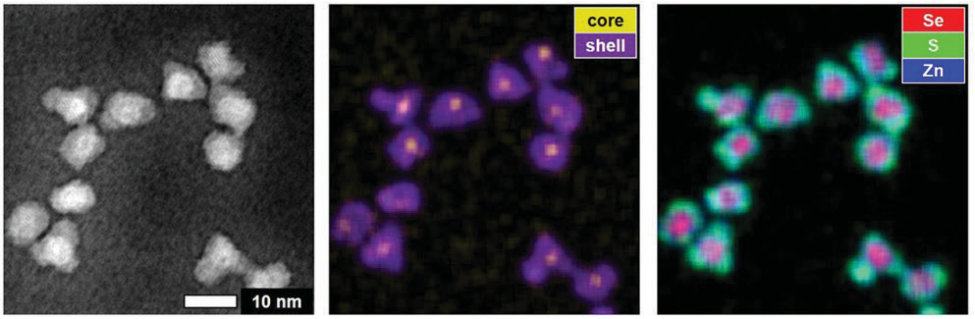


Figure 11. Low-kV S/TEM enhances microstructural imaging of nanoparticles. (Image from doi.org/10.1038/s42256-020-00289-5)

Semiconductor QDs range from to 2 to 10 nanometers, and the size determines the emitted color. Thus, particle size and distribution are critical success factors. For measurements and characterization, a high efficiency TEM with low accelerating voltage is a powerful tool for research and development during the formulation and engineering of nanoparticles (**FIGURE 10**).

It's also important to understand the core/shell structure of nanoparticles (**FIGURE 11**). However, it should be noted some QDs are beam-sensitive, and extended exposure can damage QD materials. In such cases, the most effective approach uses fast, low-dosage measurements to extract the most information in the least time while maintaining sample integrity.

Enhancing the quantum efficiency of micro-LEDs

The manufacturing of micro-LED display technology presents many challenges. One challenge described in recent literature was a process development problem where plasma etching was causing damage to multiple quantum-wells. In typical practice, plasma etching will damage multiple quantum-well structures, creating larger leakage currents that reduce the quantum efficiency of the device. To understand the extent of the damage, a dual-beam was used for site specific sample preparation at different locations, or perhaps for different crystal orientations, and a TEM was used to visualize the structure. This workflow enabled the manufacturer to characterize the damage from the plasma etching process and make process modifications.

Conclusion: Optimizing the Present and Accelerating the Future

It is an exciting time for displays with opportunities in new markets, new applications and new form factors. While mainstream technologies are not new, there is still a need for process monitoring and quality control solutions. For next generation display technologies, new materials and structures bring new challenges that require acquisition of images faster without damaging sensitive materials. Process metrology, failure analysis, and core-structure characterization can be invaluable in accelerating research and development, enhancing yield and improving display quality.

Continued from page 15

equipped with dated equipment.

"If we go back to the 2000s, Intel was an execution machine, coming out with a new node every two years like clockwork. And about every four years, they introduced some new innovation that really impacted the whole industry," Jones said. He recalled consulting with a major semiconductor vendor on the high-k metal gate development effort. A colleague called Jones up to say, "'this high-k metal gate, nobody can do this. We're working on it, but it's years away.' And like a week later, Intel introduces it in production. And for three years, they were the only one who had it."

Sanjay Natarajan: 18A node is ahead of schedule

However, the foundries "were focused on doing smaller jumps more frequently, and that allowed them to learn more quickly."

Jones said Intel has catching up to do in EUV. "I've been doing a lot of work looking at the supply and demand in EUV tools. What I think will be a particular issue for Intel is that the semiconductor industry needs about 20 more EUV tools than ASML can make in each of the next few years. Intel has the fewest EUV tools of the Big Three, so they are probably going to have the most trouble getting enough EUV tools."

Gordon Moore, now 93 years old and retired in Hawaii, must be smiling as he reads about the engineering innovations going on now in the semiconductor industry, ranging from materials such as dry forms of EUV photoresist to innovations such as TSMC's move to a SiGe channel for the PMOS devices, Samsung's early shift to a GAA architecture, and Intel's plans for PowerVia, among many others. The big jumps in transistor density may be difficult going forward, but there are enough gains to be had in performance, density, and power to say that Moore's Law is continuing, albeit in a modern form.

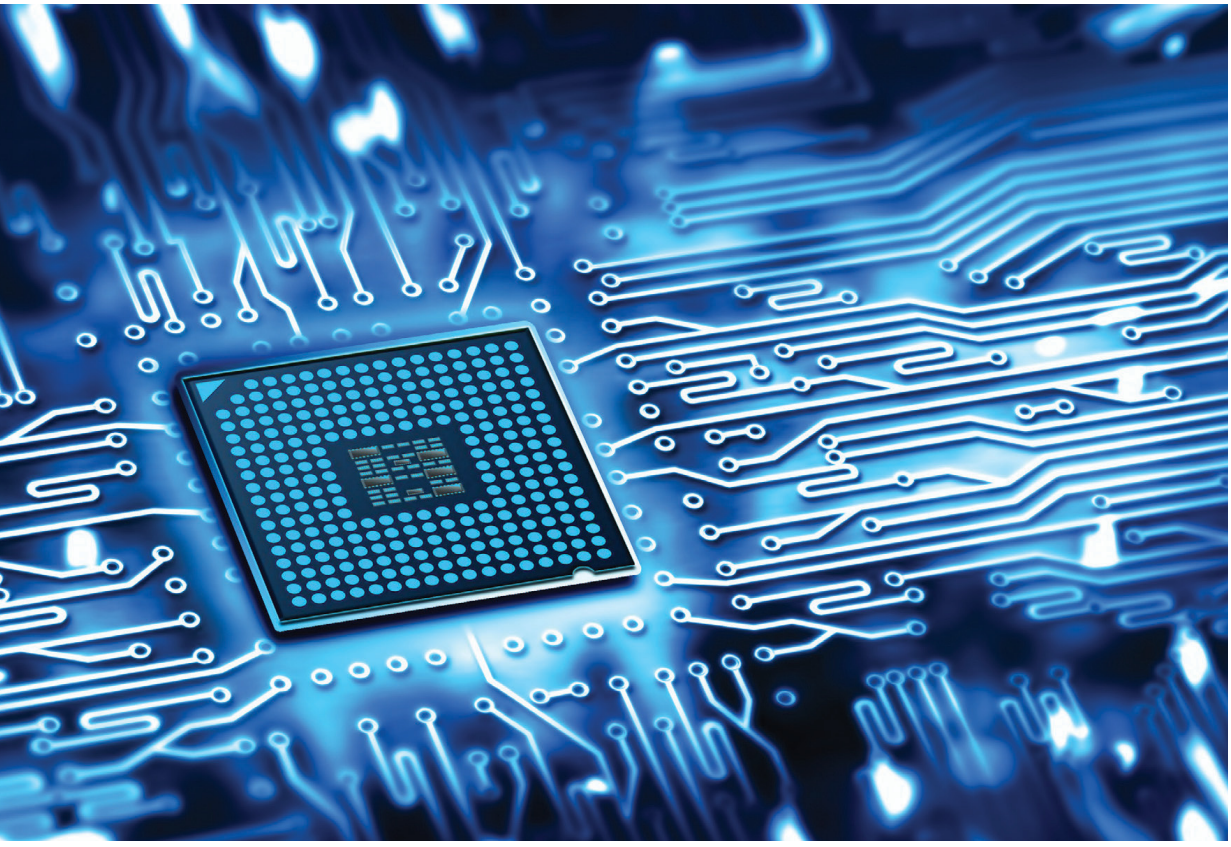
Beyond Semiconductor Packaging Materials: Advanced Silicone Solutions

JAYDEN CHO, Global Segment Leader at Dow, Korea

Advanced silicones are enabling semiconductor manufacturers to address a variety of challenges.

THE SEMICONDUCTOR INDUSTRY NEEDS TO support devices with faster operating speeds, greater densities and higher temperatures in smaller, thinner and less expensive packages. Choices for semiconductor packaging materials typically include metal, glass, plastic and ceramic; however, there are also other types of durable and functional materials to consider. For example, adhesives, coatings and encapsulants are used for thermal management, die attachment and environmental sealing applications, and for protection against shock and vibration. Yet, some chemistries may be unable to meet the increasingly challenging requirements faced by device designers, especially for electronics, telecommunications and automotive applications.

To meet these growing challenges, and to support greater production efficiency and lower energy usage, the semiconductor industry can leverage a range of advanced silicone solutions. Dependable materials such as silicone die-attach films, silicone hotmelt products and next-generation silicone-organic hybrids all provide greater performance, durability, uniformity and processability than traditional organics such as epoxies. Advanced silicone materials also provide excellent high-temperature resistance, greater temperature stability, broader and more durable adhesion and reduced risk of ionic contamination. In addition, silicones support automated production, can use energy-efficient curing methods and are available in formulations that support corporate sustainability initiatives, a consideration for investors who evaluate environmental, social and governance (ESG) performance.



Across today's increasingly competitive and expanding electronics industry, the high heat associated with 5G and its greater power densities is a growing concern. For semiconductor manufacturers, the use of integrated packages also presents heat-related challenges. There are a number of causes for semiconductor device stress, but heat is especially problematic because high temperatures can cause electronics to fail prematurely or perform unreliably. Heat can also cause secondary stresses that degrade device performance over time or result in sudden failure.

In semiconductor packages with larger chips, active device switching can produce localized hotspots that change the stress profile across the entire chip. Thinner chips can warp, and stress related problems such as die cracking, underfill material delamination and package warping may occur.

Today's integrated circuit (IC) designs support multi-function chips in both side-by-side (2D) and stacked (3D) arrangements. With 3D ICs, stacked dies need a longer path to dissipate heat; however, as the top die disperses its heat, some of this heat moves to the die below, which also requires heat dissipation. This heat transfer imparts stresses to the bottom die that can result in cracking within the entire package. Advanced silicones can relieve these temperature-induced stresses and are also a great choice for devices, such as hybrid ICs, that use materials with very different coefficients of thermal expansion (CTE) – the rate at which a material expands when heated and contracts when cooled.

Silicones are synthetic elastomers that deform rapidly when heated and then return to their original dimensions when cooled. By contrast, epoxies remain rigid and are prone to cracking because of their higher modulus of elasticity – a measure of resistance to elastic deformation when stress is applied. With their broad temperature resistance and lower modulus, reliable silicones provide better stress management while resisting the thermal cycling that can occur when chips are repetitively cycled from very low to very high temperatures, such as in power semiconductors with their higher voltages and currents.

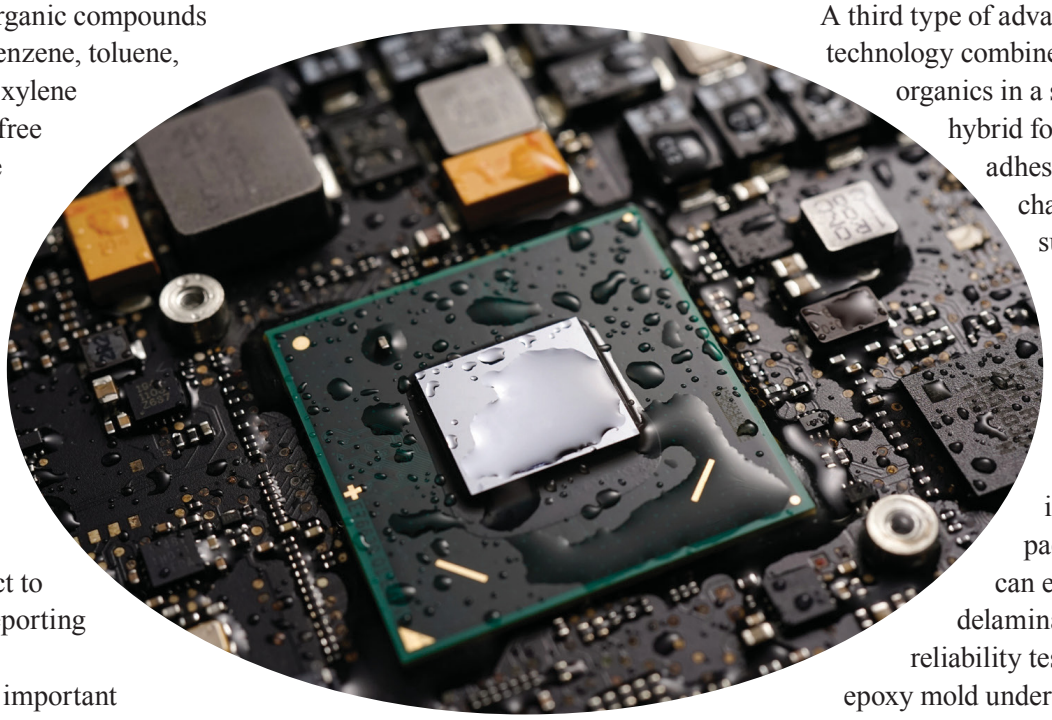
Importantly, advanced silicones provide broad and durable adhesion to a variety of semiconductor device materials, including the glass, ceramics, metal and plastics used in packaging. Advanced silicones can also bond dissimilar materials together, such as metal to plastic or glass, to support increasingly complex packaging requirements. Semiconductor devices are not used in isolation, however, and the entire thermal environment during device fabrication and printed circuit board assembly (PCBA) can be complex. Heat sinks, wires, interconnects, sensors and the PCB substrate itself can be made of various materials, each with a different CTE. Semiconductor manufacturing and PCBAs can also introduce ionic contamination, small amounts of which can cause erosion, electromigration and shorting.

Although various cleaning methods are used to remove ionic residues, wafer impurities and process particulates remain major causes of semiconductor device failure. Advanced silicones have low levels of ionic impurities and vastly help to reduce the risk of this type of contamination with benefits that include lower scrap rates and greater device reliability. Silicones also resist dust, sunlight, water and airborne contaminants. In addition, advanced silicones support the use of automated or semi-automated production equipment, such as needle dispensers or jet dispensers, for faster throughputs. In semiconductor applications such as 5G communications and automotive electronics, support for automation is important because semiconductor devices typically are manufactured in large batches.

Along with much greater assembly efficiency, advanced silicones can support reduced energy usage during curing, the chemical process that converts materials to a solid and supports desired end-use properties. There are four main curing methods for advanced silicone adhesives: evaporative, moisture, heat and ultraviolet (UV) light. Evaporative curing and moisture curing occur under ambient conditions and do not require the use of powered equipment such as ovens. Thermal curing uses infrared lamps or thermal ovens to initiate or accelerate curing. UV curing uses a UV light source instead of a thermal oven and, typically, a secondary curing mechanism.

Advanced silicones that use thermal curing are now available with lower

cure temperatures for greater energy efficiency. There are also room-temperature curing silicones where lower-temperature heat can be applied to accelerate curing. Both the heat-curing and UV-curing silicone adhesives can come in solvent-free formulations that greatly reduce or eliminate emissions of volatile organic compounds (VOCs) such as benzene, toluene, ethylbenzene and xylene (BTEX). Solvent-free materials promote environmental health and safety while helping to reduce the risk of fire because many solvents are flammable or combustible. Solvents are also closely regulated and may be subject to greenhouse gas reporting requirements.



There are other important reasons to use silicones with semiconductor devices as well. Chips are not perfectly flat, but silicones can be self-leveling or designed to self-level for a flat, even surface. Silicones' elongation and compression properties provide protection and cushioning against shock and vibration, conditions that are common in applications ranging from laptop computers and cellphones to the sensing, safety, power management and display modules used in cars. Because the density of polydimethylsiloxane (PDMS) polymers is low at approximately 1.0 g/ml, advanced silicones can also support lightweight device designs. They are a good choice for thinner packages and can also support smaller packages with higher densities of on-chip components.

There have been many recent advances in silicone technology, but materials such as silicone die-attach films (DAF) are of particular interest to the semiconductor industry. These thin, quick curing materials are used along with wire bonding, which forms an interconnection between a chip to a substrate, a substrate to a substrate or a substrate to a package. Compared to pastes, films are easier to apply uniformly across a substrate and in smaller spaces. With their well-balanced properties, silicone DAFs support thinner and more uniform bond lines without bleed-out, a common issue with epoxy adhesives. Applications include 3D stacked packages and miniaturized, high-density and multi-die packaging.

Advanced silicones are also widely used in hot melt technologies that provide excellent adhesion to a variety of substrates and stress relief for mitigating temperature-induced warpage. These advanced materials also support more efficient processing. Today, the semiconductor industry can confidently choose silicone hot melts in film, cartridge or tablet formats. Hot melt films can be vacuum laminated for large-area chip encapsulation or bonding; both processes are simpler than molding. Hot melt cartridges support compression molding, which provides better workability and thermal stability than commercial liquid-silicone encapsulants, which are used for chip encapsulation and soft molding. Hot melt tablets are designed for transfer molding and provide properties similar to conventional epoxy molding compounds (EMCs) along with exceptional thermal stability to at least 250°C.

A third type of advanced silicone technology combines silicone and organics in a specialized hybrid formulation. These adhesives deliver mechanical properties, such a higher modulus of elasticity, than silicones alone can achieve. Potential applications include flip-chip packaging, which can experience delamination after harsh reliability testing when an epoxy mold underfill is used. These silicone-organic hybrid solutions also feature excellent optical properties, enabling them to be used in optical semiconductor devices such as light-emitting diodes and photodetectors.

With their consistently well-balanced properties, advanced silicones are enabling semiconductor manufacturers to address a variety of challenges as they seek to support devices with faster operating speeds, greater densities and higher temperatures in smaller, thinner and less expensive packages. These innovative materials are also enabling faster production throughputs that use less energy for curing and that can support sustainability initiatives. As the chip shortage continues and device reliability becomes increasingly important to consumers and product manufacturers alike, advanced silicones are well-positioned to support both today's design challenges and tomorrow's packaging trends. SD

Six Steps to Realign Semiconductor Supply Chains to Seize Historical Growth Opportunities

VISHAL TALWAR, Head of High Tech, Semiconductor & Consumer Electronics, and **JOHN WAITE**, Vice President, Global Supply Chain, Genpact

The industry must fundamentally change the way functions and processes are run and how technology is employed to extract more from the current manufacturing capacity.

IT'S GOOD NEWS WHEN DEMAND FOR YOUR product skyrockets — unless, of course, you can't meet the demand.

According to the Semiconductor Industry Association, global chip sales surged 26.2 percent last year. Still there were shortages in industries ranging from the automotive sector to consumer electronics. With sales expected to rise another 8.8 percent this year, industry players are looking for solutions.

To keep pace with rising demand, the industry must fundamentally change the way functions and processes are run and how technology is employed to extract more from the current manufacturing capacity.

Here's why. The shortages were created by a perfect storm. First, semiconductors are at the heart of corporate digital transformation projects that are reinventing the way we work and live. IoT, cloud-based models, artificial intelligence and Big Data are maturing and converging to change the world as we know it. Then the pandemic struck, shutting down factories and disrupting supply chains.

JOHN WAITE

This confluence of elements has revealed deep fractures in what had been assumed to be well-aligned and performing supply chains. Systems and capabilities that were designed for a far different industry velocity are just not able to keep pace. Companies were attempting to address the problem of too much process and technology debt by throwing people at it; and that is not enough to support the current situation.

VISHAL TALWAR

Additionally, industry dynamics within the semiconductor value chain are changing. We're seeing foundries working directly with consumer electronics, fabless models moving inside traditional IDM (integrated design manufacturer) and ODM (original design manufacturer) firms, and channel partners becoming more integral to many new areas. Each of these shifts requires companies to develop new operational muscle and reorganize existing processes and systems.

As a first step to cope with this onslaught of change, semiconductor companies need to adopt enterprise-wide thinking, which leverages data driven analytics, and decision support processes and tools to prioritize for the best possible business results. Enterprise-wide thinking breaks down silos. It provides insights across the company and partner ecosystems to help semiconductor manufacturers realign supply chain frameworks in a way that enables agile teams to thrive in today's

accelerated and constantly changing environment.

Integration, finally

Perhaps most importantly, it enables true integration. Companies have been growing — organically as well as through mergers and acquisition. And growth creates a need for integration of organizational processes, systems and data – particularly around supply chain, finance, and sales ops.

While there has been no shortage of integration activities in semiconductor companies, previous investments in technology have often failed to integrate technology landscapes such as supply chain networks and infrastructure as well as multiple ERP, planning, and data systems. As a result, any residual problems around master data such as unclean data, data duplicates, or data inconsistencies can cause serious challenges in planning, manufacturing, procurement, and fulfilment.

The solution? Firms must allocate resources, integrated planning, and analytics far more efficiently and effectively.

Sometimes that's easier said than done. Complicating matters are decades of outsource models with lack of cross-company integration and control tower gaps. Given the interdependence of the semiconductor industry, a lot of businesses rely on other companies in the ecosystem to execute their networks and supply chains. This has caused serious issues around core supplier integration and visibility, and in some cases, has led to major business disruptions hampering growth opportunities. Some companies are literally waiting to see what shows up on their docks to figure out what they can build.

Finally, the semiconductor industry must cope with enormous risk across the spectrum of geopolitical problems, natural disasters, labor challenges, IP restrictions, environmental mandates and an ever more dependent, but often not visible, ecosystem. As such, firms are turning to their traditional planning processes to evaluate risk scenarios, but often find incomplete data and analytics, and a lack of talent to rapidly assess, react, and mitigate risk.

A supply chain framework to accelerate business velocity

By analyzing and realigning supply chain frameworks, semiconductor manufacturers can identify people, process, technology, and data obstacles that are causing design, manufacturing, and delivery bottlenecks. Organizations can then more rapidly assess and seize the market opportunities that will bring wins and impactful outcomes via short period sprints.

Semiconductor manufacturers can achieve this with the following six-step methodology that has been implemented successfully in enterprises across the globe:

1. **Project alignment:** Start by collecting and analyzing existing data; assessing the processes, technology, data, and organization as it stands. Next, align stakeholders and communicate goals to create a detailed project plan and mobilization activities.
2. **Assess vision and current state:** Evaluate how vision, strategy, and business case ambitions align, as well as the capabilities required to achieve the vision. Use this to define the design principles for the target operating model, identifying regional archetypes to segment the operating model.
3. **Process design:** Define the process enablers required for capabilities and develop processes to support customer centric thinking. Document collaboration points and functional handoffs; and set master data management process cadence with planning cycles.
4. **Digital architecture:** Next, assess the as-is technology landscape to define the technology enablers required for achieving capabilities, and develop a high-level technology and data architecture based on archetypes.
5. **Organizational design:** Define the organizational enablers required for new capabilities and conduct location analysis. Define the organizational model, develop user journeys across processes, and identify the skills and capabilities needed to operate the new model.
6. **Define the roadmap:** Finally, design an implementation roadmap by defining the resource requirements for implementation. Architect the transformation program and governance, estimate the benefits and cost of implementation, and build business case scenarios.

At a time when the semiconductor industry is experiencing extraordinary growth and extraordinary challenges, enterprise-wide thinking helps companies tackle both by breaking down silos and realigning supply chains. Relieved of costly bottlenecks, companies are then ready to scale rapidly, capture opportunities, and drive growth.

About the authors

Vishal Talwar leads the High Tech (Enterprise Technology), Semiconductor & Consumer Electronics business for Genpact. Genpact (NYSE: G) is a global professional services firm focused on delivering digital transformation. Vishal and his team drive growth, effectiveness and value for both existing and new clients.

As Vice President, Global Supply Chain, John Waite leads business development and transformation, helping Genpact clients solve global supply chain challenges. He advises clients on cost effective procurement, vendor and supplier management.

Achieving ISO/SAE21434 Cyber Security Using Secure Flash

NIR TASHER, Director of Technology, Winbond Security Products

The new standard requires the automotive industry to adapt devices capable of meeting this standard and provide the required protection against cyber threats.

MODERN CARS TODAY CONTAIN dozens of computerized modules executing billions of instructions every second. These modules perform diverse tasks from monitoring tire pressure, controlling suspension and steering, applying and monitoring breaks, to advanced driver assistance systems like navigation and entertainment.

Network connectivity in modern cars should be ubiquitous, connecting the multitude of car subsystems essential for performing remote diagnostics, connecting with traffic networks, allowing media streaming and navigation, and providing access to the car vendor for routine software updates. This connectivity can be Wide Area (WAN) or local, within the car or in the proximity of the car. The car owner is rarely aware of this high level of connectivity or the possibility of an attacker gaining access to the many connected systems from afar. Physical access to a module or car can be assumed during the vulnerability discovery phase, but the actual attack is often mounted from a remote location.

Network connectivity opens a multitude of cyber threats to cars, allowing hackers to perform penetration attempts into car systems, execute malicious code and place vehicle users and pedestrians at risk of severe injuries. Theft of data can jeopardize the car owner, the manufacturer, and the infrastructure.

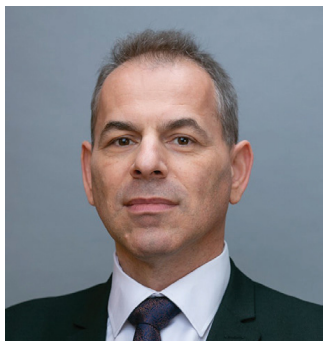
ISO/SAE21434 specifies the requirements for making a car system more robust against cyber-attacks. It outlines the criteria during the concept, development, production, usage and decommission of automotive systems. The requirements of ISO 21434 apply to systems, subsystems and components whose development started after the publication of the standard in August 2021.

ISO21434 has been made mandatory by many car makers and their component suppliers, starting from mid-2022. As a result, the automotive industry is now required to significantly improve how cyber threats are managed. As this standard applies to both the modules and their components, it requires the automotive industry to adapt devices capable of meeting this standard and provide the required protection against cyber threats.

One of the critical components of the electronic modules in car systems is the non-volatile memory, namely the Flash device. This device holds the entire code of the microcomputer and most of the security-critical data such as ID, security keys, user data etc. The Flash thus becomes the target of hackers who will try to extract information from it and modify the content in order to modify the code, erase keys, overwrite keys to a known default value, or modify user data and system ID. Such

Figure 1. Winbond's secure Flash supports end to end encrypted updates while preventing 3rd party hacking attempts.

attacks have dangerous consequences ranging from car immobilization and car theft to loss of control during high-speed cruising — or even taking down complete infrastructures by executing Distributed Denial of Service (DDoS) attacks.



NIR TASHER

The majority of focus in handling cyber-attacks goes into preventing unauthorized access and modification of the flash content while allowing the content of the Flash to be updated, usually using a remote Over the Air (OTA) update mechanism. All the protection, access and update mechanisms must work coherently to maintain the system security. However, in most cases, this is an unrealistic goal. To make matters even more complex, the sheer effort of obtaining ISO21434 certification for such complex and multi-layered software can be overwhelming.

ISO21434 mandates software updates as a reaction to identified security vulnerabilities. The software updates need to be urgent and cannot rely solely on shop recalls. They must be pushed directly to the cars via OTA. Such updates will become very frequent and rely on a secure mechanism to carry them out.

The certified secure Flash device family from Winbond was designed from the get-go to simplify the process of taking standard systems and bolting on security in a practical and transparent way. The drop-in replacement secure Flash can increase the security level of any existing or new design with minimal to no change of the system software. The hardware-based design of the secure Flash guarantees that it cannot be modified or hacked. The secure Flash devices from Winbond are fully certified to the most stringent security standards, including CC EAL5+, EAL2 and ISO21434. Winbond facilities are certified for secure product development and production at the highest security level.

The secure Flash handles operations such as:

- Root of Trust
- Boot security with automatic fall-back code remapping
- Roll-back protected end-to-end secure and encrypted firmware update with built-in fail-safe.
- Section-based cryptographic write protection
- Per section access control including encrypted read and write
- Secure, encrypted Storage
- Data signing mechanism using on-chip keys that are not user-accessible
- Monotonic counters
- Secure watchdog

When used according to Winbond's guidelines, these operations prevent malicious attacks on the system and make the system resilient to errors and faults. The secure Flash operation is implemented in hardware. Winbond supplies an open-source code support library for quick and straightforward user integration.

With the above operations implemented, the microcomputer operation in submodules is made secure and compliant with ISO21434 requirements — preventing malicious attacks from compromising subsystems in the car.

Winbond is the only vendor of security certified Flash devices. Their secure flash products for automotive are ISO26262 safety certified, offering Automotive Grade quality assurance.

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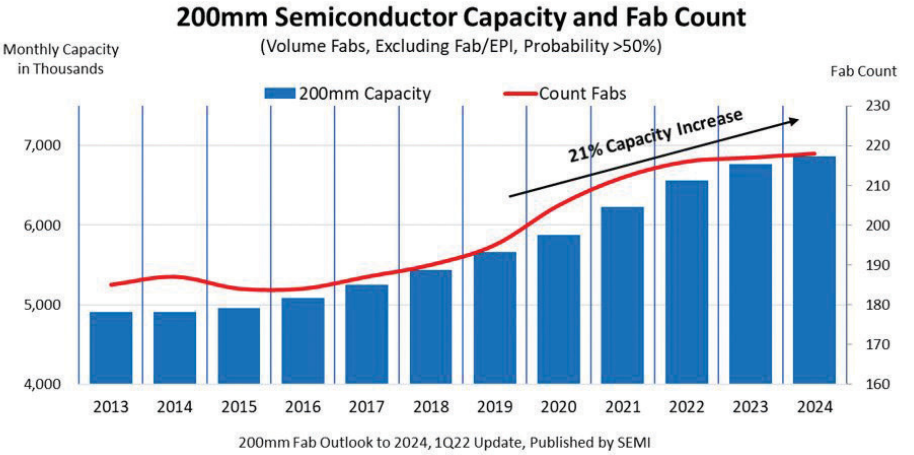
200mm Semiconductor Fab Capacity Set to Surge 21%

Semiconductor manufacturers worldwide are on track to boost 200mm fab capacity by 1.2 million wafers, or 21%, from the start of 2020 to the end of 2024 to hit a record high of 6.9 million wafers per month, SEMI announced in its 200mm Fab Outlook Report. After climbing to $5.3 billion last year, 200mm fab equipment spending is expected to be $4.9 billion in 2022 as 200mm fab utilization remains at high levels and the global semiconductor industry works to overcome the chip shortage.

"Wafer manufacturers will add 25 new 200mm lines over the five-year period to help meet growing demand for applications such as 5G, automotive and Internet of Things (IoT) devices that rely on devices like analog, power management and display driver integrated circuits (ICs), MOSFETs, microcontroller units (MCUs) and sensors," said Ajit Manocha, SEMI president and CEO.



200mm installed semiconductor capacity and fab count, 2013 to 2024. Fab count is net of wafer-size conversions. *Source: SEMI*

The SEMI 200mm Fab Outlook Report, covering the 12 years from 2013 to 2024, also reveals that foundries will account for more than 50% of fab capacity worldwide this year, followed by analog at 19% and discrete/power at 12%. Regionally, China will lead the world in 200mm capacity with 21% share in 2022, followed by Japan with 16% and Taiwan and Europe/Mideast at 15% each.

Equipment investments are projected to remain above $3 billion in 2023, with the foundry sector accounting for 54%, followed by discrete/power at 20% and analog at 19%.

The SEMI 200mm Fab Outlook Report lists more than 330 fabs and lines and includes 64 changes across 47 fabs since its most recent update in September 2021.

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Adding More to Moore's Law

DR. BELGACEM HABA, Senior Technical Fellow and Vice President of Path Finding Team, Xperi

IT IS A QUOTATION STRAIGHT FROM CHARLES Dickens "please sir may I have some more?" Today it sums up an attitude to technology – can I have more features, more speed, more memory, more time – and also pay less? Little wonder that Moore's Law is one of technology's most oft-quoted maxims.

But of course, Moore's Law was never a real law. It was a prediction originally made by Gordon Moore, Intel's co-founder, more than 50 years ago in 1965. He observed that as transistors became smaller, the number that could fit on a single-layer silicon chip would double every two years or so, and therefore so would its computing power. As a prediction, Moore's Law turned to be surprisingly accurate.

In a sense, it even became a self-fulfilling prophecy as all the parties in the manufacturing chain effectively accepted it as the goal and collaborated to make it a reality. But in terms of its original sense and definition, there's little doubt that Moore's Law is close to reaching its achievable limit, and progress has slowed considerably in the past decade.

A restated version of Moore's Law might argue that while the scope of what embedded technology can achieve in performance terms continues to grow, the price of delivering that performance continues, in real terms, to fall. Twice the performance at half the price might, in fact, be the next goal but progress towards that will continue to be driven by Moore's Law-style innovation and the improvements in performance that we can achieve.

Since its origin, Moore's Law has been defined primarily by the transistor — how many could we fit on any given unit. But once a transistor reaches one atom in width, a reality getting closer every day, it's physically impossible to make it any smaller and to add any more to a single chip. So, what if we redefine the implications of Moore's Law and say that the number of transistors alone doesn't matter. What matters is the performance of the system.

3D integration of multiple electronic components stacked together means they can act as a single entity, requiring less power but also allowing more features and performance capability without compromising device size or battery life – in fact there is a likelihood of a reduction in size where desirable.

Known as hybrid bonding 3D interconnect, or hybrid interconnect, this approach has the potential to expand the horizon of Moore's Law. In this model, instead of a single layer of transistors on a silicon wafer, additional layers are built and stacked on top of each other, finding ways to connect them vertically as well as horizontally. Adeia invented and pioneered a hybrid bonding technology referred to as DBI (direct bond interconnect) that dramatically increases the number of vertical connections between these two surfaces.

With DBI technology, transistors in an active chip also see the transistors in the chip above and below, just as they would if they were sitting within the same chip. DBI works by taking two silicon chips with exposed contacts on both sides and joining them together so that the parts fuse at a relatively low temperature. The finished product might look like a stacked chip but it functions as a "single layer" chip.

As these chips become more powerful and more commonplace, they will create bandwidth that is unimaginable using any other configuration or technique - especially given their power efficiency. Within each of these chips, each transistor is constantly sending and receiving billions of transmissions. If these elements were spread horizontally rather than stacked vertically, the signals would have to travel much further and require far more power.

Just a few short years ago, many in the industry were worried that Moore's Law was coming to an end. These innovations open-up a new way of thinking about the Law meaning we can continue to increase processing capability – maybe for as long as the next 50 years. By looking up, we have been able to add more to Moore's Law, with a vertical definition that extends its life for the next wave of innovation.

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